Sample Questions

Information Technology

Subject Name: Computer Organization and Architecture **Course Code**:ITC405

Semester: IV

Multiple Choice Questions

	Choose the correct option for following questions. All the Questions carry equal marks
1.	What is the 2's complement of 0010 ?
Option A:	1101
Option B:	0101
Option C:	1110
Option D:	1010
2.	-------- is a circuit with many inputs and one output.
Option A:	DECODER
Option B:	MUX
Option C:	ENCODER
Option D:	DEMUX
3.	-- is used as a building block of memory.
Option A:	Half Adder
Option B:	MUX
Option C:	Encoder
Option D:	Flip Flop
4.	What is the result of 10100 - 00101 ?
Option A:	01111
Option B:	01010
Option C:	10000
Option D:	00101
5.	If the program has a total 1000 instructions and CPU has 10 average CPI with speed of 2GHz. Find the execution time of a program
Option A:	01 micro seconds
Option B:	50 micro seconds
Option C:	05 micro seconds
Option D:	10 micro seconds
6.	Assuming AL=00H, which flag will be set when ALU performs, SUB AL, 22H?
Option A:	Sign
Option B:	Carry
Option C:	Parity
Option D:	Zero

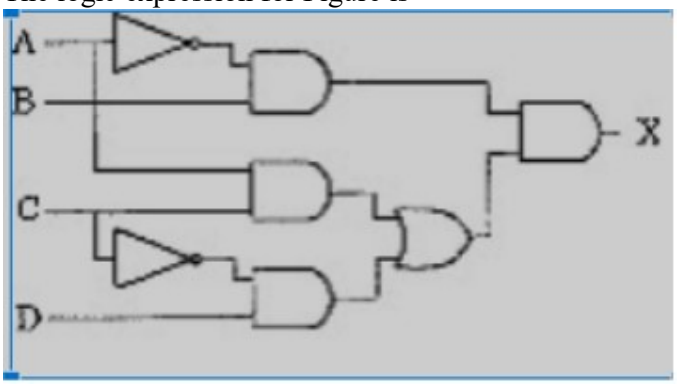
7.	MOV [1050H], BL is an example of _____ addressing mode.
Option A:	Indirect
Option B:	Register
Option C:	Direct
Option D:	Implied
8.	_____ is not a conditional jump instruction.
Option A:	JC
Option B:	JNC
Option C:	JMP
Option D:	JNZ
9.	If the initial value of AL register is 55H, what is the value stored in AL register after the execution of AND AL, 0FH?
Option A:	00H
Option B:	50H
Option C:	55H
Option D:	05H
10.	During the execution of an instruction, the processor checks for an interrupt ----- .
Option A:	As soon as an interrupt occurs
Option B:	After fixed time interval
Option C:	Will not check during instruction execution
Option D:	After the current instruction execution
11.	------- is used to control the hardware of the system.
Option A:	Programming
Option B:	Microprogramming
Option C:	Assembly programming
Option D:	Nanoprogramming
12.	Which is not the part of CPU?
Option A:	ALU
Option B:	Flash memory
Option C:	Registers
Option D:	Control Unit
13.	---- register stores internally the address of memory location to be accessed for read/write operation.
Option A:	MDR
Option B:	SI
Option C:	MAR
Option D:	AX

14.	In case of Non Restoring Division Algorithm, when 18 is divided by 10, then what is stored in the registers Q & A respectively ?
Option A:	0001 , 1000
Option B:	0110 , 0001
Option C:	1000, 0001
Option D:	0001, 1010
15.	How many bits are used to represent "Exponent" in Single precision IEEE 754 floating point standard?
Option A:	8
Option B:	127
Option C:	32
Option D:	16
16.	If cache memory has 10 lines, then 24th block of main memory would be placed in which line of cache memory, in case of direct mapping function?
Option A:	1
Option B:	2
Option C:	3
Option D:	4
17.	In the memory hierarchy, -------- is most nearest to the processor.
Option A:	Register
Option B:	DRAM
Option C:	Cache
Option D:	SRAM
18.	Which system faces the problem of cache coherency?
Option A:	Client-server
Option B:	Multi-processor
Option C:	Multi-tasking
Option D:	Single bus
19.	I/O module sends a signal to CPU when device is ready, this is called as_____
Option A:	Interrupt driven I/O
Option B:	Exceptions
Option C:	Signal handling
Option D:	DMA
20.	In case of ----, the I/O devices and the memory devices have the same address space in memory .
Option A:	IO mapped-mapped I/O
Option B:	Interrupt-driven I/O
Option C:	Memory-mapped I/O
Option D:	Direct Memory Access
21.	Memory mapped I/O means

Option A:	Using separate memory address space for I/O ports
Option B:	Assigning a part of the main memory address space to I/O ports
Option C:	Using separate input and output instructions
Option D:	Using combined input and output instructions
22.	Instruction AND is executed by
Option A:	Decoder unit
Option B:	ALU
Option C:	Memory unit
Option D:	Control unit
23.	In memory Hierarchy which is the fastest memory
Option A:	SRAM
Option B:	DRAM
Option C:	Register
Option D:	Cache
24. Cache memory is also known as	
Option A:	Content Addressable Memory
Option B:	Content Accessible Memory
Option C:	Computer Addressable Memory
Option D:	Computer Accessible Memory
25.	Micro program consisting of _____ is stored in control memory of control unit
Option A:	Instructions
Option B:	micro instructions
Option C:	micro program
Option D:	macro program
26.	Choose appropriate sequence of instruction cycle
Option A:	Instruction fetch, Instruction address calculation, Instruction decode, operand address calculation , fetch operand, data operation, operand address calculation, operand store
Option B:	Instruction address calculation , Instruction fetch, operand address calculation fetch operand, Instruction decode, data operation, operand address calculation and operand store
Option C:	Instruction address calculation , Instruction fetch, Instruction decode, operand address calculation , fetch operand, data operation , operand address calculation, operand store
Option D:	Instruction address calculation, Instruction fetch, Instruction decode, operand address calculation , fetch operand, operand address calculation , operand store, data operation
27.	In Instruction Pipelining Structural Hazard means
Option A:	any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline
Option B:	a delay in the availability of an instruction causes the pipeline to stall

Option C:	the situation when two instructions require the use of a given hardware resource at the same time.
Option D:	When a data gets overwritten by branching
28.	Convert number($41.62)_8$ into equivalent hexadecimal number
Option A:	$(20.D8)_{16}$
Option B:	$(21.C8)_{16}$
Option C:	$(21.D8)_{16}$
Option D:	$(20.C8)_{16}$
29.	The sign and magnitude representation for +7 is
Option A:	00001000
Option B:	10000101
Option C:	10000111
Option D:	00000111
30.	8086 has 20 bit address lines to access memory, hence it can access
Option A:	100 MB
Option B:	1 KB
Option C:	1 MB
Option D:	10 MB
31.	The advantage of DMA is
Option A:	Avoiding busy waiting by CPU
Option B:	High speed data transfer between memory and I/O
Option C:	Polling
Option D:	Accessing CPU
32.	Program Counter Holds
Option A:	The Instruction
Option B:	The Data
Option C:	Address of the Current Instruction which is executed
Option D:	Address of the Next Instruction to be executed
33.	Which of the following is not a key characteristics of memory devices or memory system
Option A:	Location
Option B:	Physical Characteristics
Option C:	Availability
Option D:	Access Method
34.	In restoring division method when subtraction is said to be unsuccessful
Option A:	if result is positive
Option B:	if result is negative
Option C:	if result is zero
Option D:	if result is infinite

35.	The disadvantage of an SRAM is
Option A:	Very high power consumption
Option B:	Very high access time
Option C:	These are volatile memories
Option D:	Very low price
36.	The main memory contains 8K blocks, each consisting of 128 words. How many bits are there in a main memory address?
Option A:	19 bits
Option B:	21 bits
Option C:	22 bits
Option D:	20 bits
37.	In Restoring division Algorithm if A<0 then which of the following is immediate step (Assume M as Dividend Q as Divisor And A as result)
Option A:	Q_0 =0
Option B:	A= A +M
Option C:	Q_0 =0 & A=A-M
Option D:	Q_0 =0 & A=A+M
38.	Third generation of computer is between
Option A:	1940 and 1956
Option B:	1964 and 1971
Option C:	1972 and 2010
Option D:	1910 and 1930
39.	Find the output of full adder with A=1, B=0, C=1
Option A:	S=0,C=0
Option B:	S=0,C=1
Option C:	S=1,C=0
Option D:	S=1,C=1
40.	A combinational logic circuit which sends data coming from a single source to two or more separate destinations is
Option A:	MUX
Option B:	ENCODER
Option C:	DECODER
Option D:	DEMUX
41.	How many two-input AND and OR gates are required to realize Y = CD+EF+GH?
Option A:	3,3
Option B:	3,2
Option C:	2,3
Option D:	2,2

42.	The hexadecimal number $(3E8)_{16}$ is equal to decimal number ……
Option A:	1000
Option B:	982
Option C:	768
Option D:	320
43	The logic expression for Figure is 
Option A:	$X = \overline{A}\overline{B}C + A\overline{C}\overline{D}$
Option B:	$X = AB\overline{C}\left(\overline{C}BD\right)$
Option C:	$X = \left(\overline{A}B\right)\left(AC + \overline{C}D\right)$
Option D:	$X = \left(\overline{A}B\right)\left(A\overline{C}\overline{C}D\right)$
44.	------ are used to convert one type of number system to another form
Option A:	Encoder
Option B:	Logic Gates
Option C:	Half Adder
Option D:	Full Adder
45.	The different ways in which a source operand is denoted in an instruction is known as
Option A:	Instruction Set
Option B:	Interrupts
Option C:	8086 Configuration
Option D:	Addressing Modes
46.	If AX = FFFFH and add AX,01h instruction is executed. The value in AX reg is
Option A:	1010 H
Option B:	1111 H
Option C:	0000 H
Option D:	0101 H
47.	Which of the following is an implicit instruction ?
Option A:	ADD

Option B:	ADC
Option C:	AAA
Option D:	ADD & ADC
48.	Match the following a) DB 1) used to direct the assembler to reserve only 10-bytes b) DT 2) used to direct the assembler to reserve only 4 words c) DW 3) used to direct the assembler to reserve byte or bytes d) DQ 4) used to direct the assembler to reserve words
Option A:	a-3, b-2, c-4, d-1
Option B:	a-2, b-3, c-1, d-4
Option C:	a-3, b-1, c-2, d-4
Option D:	a-3, b-1, c-4, d-2
49.	The condition flag Z is set to 1 to indicate _____
Option A:	The operation has resulted in an error
Option B:	The operation requires an interrupt call
Option C:	The result is zero
Option D:	There is no empty register available
50.	The Instruction fetch phase ends with _____
Option A:	Placing the data from the address in MAR into MDR
Option B:	Placing the address of the data into MAR
Option C:	Completing the execution of the data and placing its storage address into MAR
Option D:	Decoding the data in MDR and placing it in IR
51.	A shared communication path consisting of one or more connection lines between registers is known as
Option A:	Transistor
Option B:	Integrated Circuits
Option C:	Bus
Option D:	Register Transfer
52.	Which of the following Special purpose register holds the operation codes currently being executed?
Option A:	Program Counter
Option B:	Instruction Register
Option C:	Stack pointer
Option D:	Base Register
53.	Transfer of data from memory to processor during load operation is done on this register
Option A:	Accumulator
Option B:	Instruction register
Option C:	Program Counter
Option D:	MAR

54.	Control Units are designed using which of the following approach?
Option A:	Hardwired approach
Option B:	Microprogramming approach
Option C:	Hardwired & Microprogrammed approach
Option D:	Macro programming approach
55.	The advantage of using Dynamic RAM as main memory in a computer system as it
Option A:	Consumes less power
Option B:	has higher speed
Option C:	has lower cell density
Option D:	needs refreshing circuitry
56.	Which of the following is example of internal processor storage component
Option A:	Registers
Option B:	Hard disk
Option C:	RAM
Option D:	ROM
57.	The memory that communicates directly after cache with CPU is
Option A:	Secondary Memory
Option B:	Primary Memory
Option C:	Shared Memory
Option D:	Auxiliary memory
58.	Unit of computer which controls processors communication with peripheral devices is called
Option A:	Control Unit
Option B:	I/O unit
Option C:	ALU
Option D:	Memory Unit
59.	The I/O Devices are also known as
Option A:	Framework
Option B:	Peripherals
Option C:	Firmware
Option D:	Software
60.	The advantage of I/O mapped devices over memory mapped is
Option A:	The former offers faster transfer of data
Option B:	The devices connected using I/O mapping have a bigger buffer space
Option C:	The devices have to deal with fewer address lines
Option D:	No advantage as such

Descriptive Questions

10 marks each	
A	Explain the memory segmentation and memory banking of 8086 Microprocessor.
B	With the help of diagram, explain 6-stage pipeline architecture and various pipeline hazards with example.
C	Explain different cache mapping techniques.
D	Draw the flow chart of Booths algorithm for signed multiplication and Perform 7 x -3 using booths algorithm
E	Explain in detail with suitable Architecture of 8086 microprocessor
F	List and explain in detail characteristics /parameters of memory
G	Explain architecture of 8086 in detail
H	Draw Booths Algorithm flowchart and solve for -9 * 9
I	Minimize the following 4 variable logic function using K- map and draw logic diagram for reduced expression: 1. f(A,B,C,D) = ∑m (0,1,3,4,7,9,11,13,15) 2. f(A,B,C,D) = πM (0,2,5,6,10,12,13,14)

5 marks each	
A	Write a program for an 8086 microprocessor to add two 8 bit decimal numbers.
B	Reduce the expression using K – Map: f(a,b,c,d) = ∑ m (2, 4, 6, 10, 11,12, 14). Also draw the logic circuit for the reduced expression.
C	Explain the working of 8:1 Multiplexer.
D	Perform the multiplication of -5 X 4 using Booth's algorithm.
E	Discuss the need of I/O module in computing system.
F	With neat diagram, explain Memory Hierarchy.
G	Explain the working of 8:1 Multiplexer.
H	Minimize the following four variable logic function using K-map f(A,B,C,D)=∑m(0,1,3,4,7,9,11,13,15)
I	Describe Flynn's classification of parallel computing in detail
J	Differentiate between Hardwired control unit and Micro programmed control unit
K	Identify the addressing modes of the following instructions 1.MOV AX,1000 2.MOV AX,[1000] 3.MOV AX,BX 4.MOV [BX],AX 5.MOV AX,[SI+200]
L	Write short note on DMA
M	Explain Flynn's Classification of parallel computers.
N	Explain IEE 754 standards for floating point representation with examples.
O	Explain different data transfer techniques of DMA.

P	Explain Amdahl's Law.
Q	Explain in short, the concept of Nano programming.
R	Give types of Cache Mapping technique and explain any one in detail