University of Mumbai

Program: **Electronics and Telecommunication Engineering**

Curriculum Scheme: Rev2019

Examination: **TE Semester V**

Course Code: **ECC503** and Course Name: **Digital VLSI**

Time: 2 hours 30 minutes Max. Marks: 80

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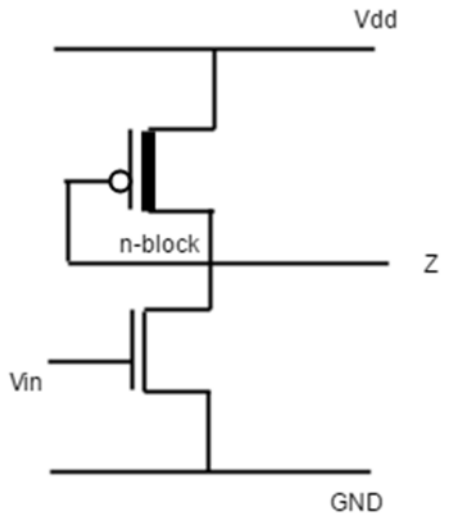
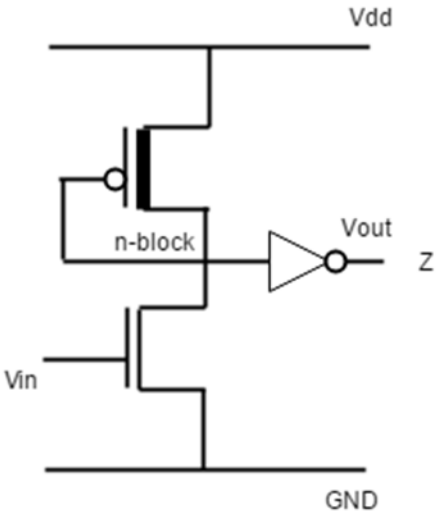
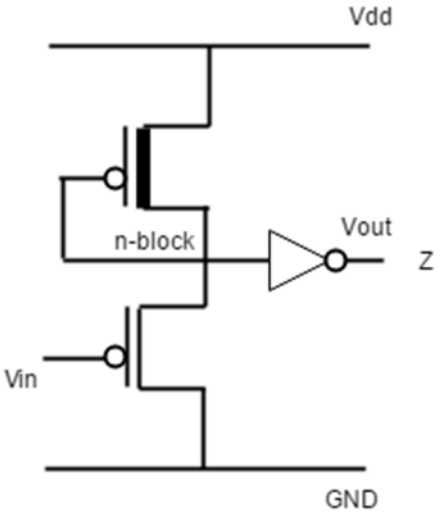
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	In Constant Voltage model, the scaling factors β and α are related as:
Option A:	$\beta = \alpha$
Option B:	$\alpha = 2\beta$
Option C:	$\beta = 1$
Option D:	$\beta = \alpha = 1$
2.	In Constant voltage model the gate capacitance is scaled by a factor of:
Option A:	$1/\beta^2$
Option B:	$1/\alpha^2$
Option C:	β/α^2
Option D:	α/β^2
3.	As the number of inputs increases, the NAND gate delay
Option A:	increases
Option B:	decreases
Option C:	does not vary
Option D:	exponentially decreases
4.	CMOS domino logic can be expressed diagrammatically as
Option A:	

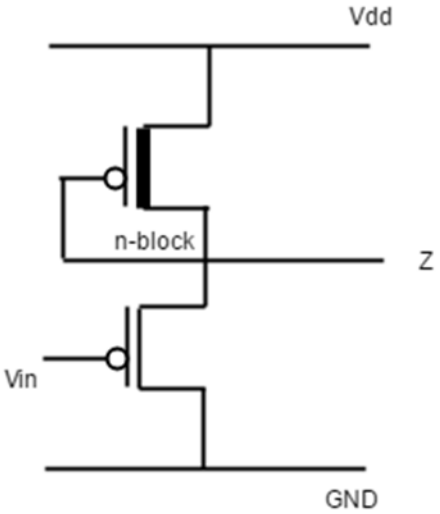
Option B:



Option C:



Option D:



5. The truth table which accurately explains the operation of CMOS NOT gate is:

Option A:

Input	pMOS	nMOS	Output
0	OFF	ON	1
1	OFF	ON	0

Option B:	<table><tr><th>Input</th><th>pMOS</th><th>nMOS</th><th>Output</th></tr><tr><td>0</td><td>ON</td><td>OFF</td><td>1</td></tr><tr><td>1</td><td>ON</td><td>OFF</td><td>0</td></tr></table>
Option C:	<table><tr><th>Input</th><th>pMOS</th><th>nMOS</th><th>Output</th></tr><tr><td>0</td><td>ON</td><td>ON</td><td>1</td></tr><tr><td>1</td><td>OFF</td><td>OFF</td><td>0</td></tr></table>
Option D:	<table><tr><th>Input</th><th>pMOS</th><th>nMOS</th><th>Output</th></tr><tr><td>0</td><td>ON</td><td>OFF</td><td>1</td></tr><tr><td>1</td><td>OFF</td><td>ON</td><td>0</td></tr></table>
6.	When both the AND & OR are programmable, such PLDs are known as?
Option A:	PAL
Option B:	PPL
Option C:	PLA
Option D:	APL
7.	In Pseudo-NMOS logic, N transistor operates in
Option A:	cut off region
Option B:	saturation region
Option C:	resistive region
Option D:	non saturation region
8.	Which type of storage element of SRAM is very fast in accessing data but consumes lots of power?
Option A:	TTL
Option B:	CMOS
Option C:	NAND
Option D:	NOR
9.	How many NOT gates are required to implement the Boolean expression: X = AB'C + A'BC?
Option A:	2
Option B:	3
Option C:	4
Option D:	5
10.	What are carry generate combinations?
Option A:	If all the input are same then a carry is generated
Option B:	If all of the output are independent of the inputs
Option C:	If all of the input are dependent on the output
Option D:	If all of the output are dependent on the input

Q2	**Solve any Two out of Three** **10 marks each** ***Please delete the instruction shown in front of every sub question***
A	*Explain NMOS FABRICATION in detail with all suitable diagrams.*
B	*Draw and explain operation of SRAM read and write circuitry in detail.*

C	*What are the various regions of operation of MOSFET? Explain in detail.*

Q3	**Solve any Two Questions out of Three** **10 marks each**
A	*Compare RTL (Register Transfer Level) design and Sequential logic design.*
B	*Explain CMOS fabrication in detail with all suitable diagrams.*
C	*Explain in detail different modes of operation of MOSFET under external bias conditions.*

Q4.	
A	**Solve any Two** **5 marks each**
i.	*Implement the equation X = ((A + B) (C + D + E) + F) G using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?*
ii.	*Compute the following for the pseudo-NMOS inverter shown in Figure:* *a. VOL and VOH* *b. NML and NMH* *c. For an output load of 1 pF, calculate tp_{LH}, tp_{HL}, and tp are the rising and falling delays equal? Why or why not?*
iii.	*Suppose we want to implement two logic functions given by F=A+B+C and G=A+B+C+D. Assume both true and complementary signals are available.* *a) Implement these functions in dynamic CMOS as cascaded stages so as to minimize the total transistor count.* *b) Discuss any conditions under which this implementation would fail to operate properly.* *c) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b)?*
B	**Solve any One** **10 mark each**
i.	*Explain stick diagram rules with color coding and draw a stick diagram for CMOS inverter.*
ii.	*Discuss about Lambda design rules in detail.*