University of Mumbai

Program: **Electronics and Telecommunication Engineering**
Curriculum Scheme: Rev2019
Examination: **TE Semester V**
Course Code: **ECC503** and Course Name: **Digital VLSI**
Time: 2 hours 30 minutes Max. Marks: 80

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Q1. Choose the correct option for following questions. All the Questions are compulsory and carry equal marks

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	B
Q3.	A
Q4	A
Q5	D
Q6	C
Q7	B
Q8.	A
Q9.	A
Q10.	B

Q2 (20 Marks Each)	**Solve any Two out of Three** **10 marks each** ***Please delete the instruction shown in front of every sub question***
A	*Explain NMOS FABRICATION in detail with all suitable diagrams.*
B	*Draw and explain operation of SRAM read and write circuitry in detail.*
C	*What are the various regions of operation of MOSFET? Explain in detail.*

Model Answer: (with marks distribution)

A. Explain NMOS FABRICATION in detail. (10 marks)
(Explanation =5 Marks and Diagrams = 5 Marks)

The following description explains the basic steps used in the process of fabrication.

(a) The fabrication process starts with the oxidation of the silicon substrate. It is shown in the Figure (a).

(b) A relatively thick silicon dioxide layer, also called field oxide, is created on the surface of the substrate. This is shown in the Figure (b).

(c) Then, the field oxide is selectively etched to expose the silicon surface on which the MOS transistor will be created. This is indicated in the Figure (c).

(d) This is followed by covering the surface of substrate with a thin, high-quality oxide layer, which will eventually form the gate oxide of the MOS transistor as illustrated in Figure (d).

(e) On top of the thin oxide, a layer of polysilicon (polycrystalline silicon) is deposited as is shown in the Figure (e). Polysilicon is used both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The resistivity of polysilicon can be reduced, however, by doping it with impurity atoms.

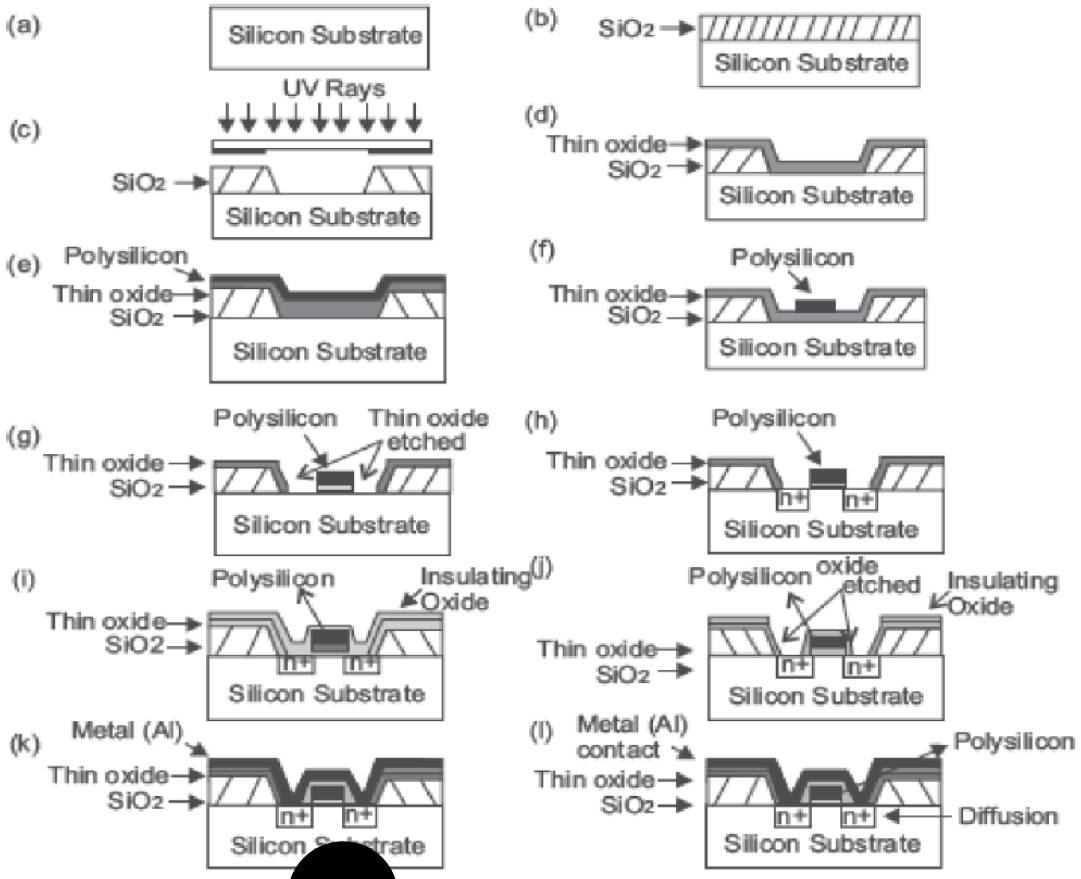
(f) After deposition, the polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gates. This is shown in Figure (f).

(g) The thin gate oxide not covered by polysilicon is also etched along, which exposes the bare silicon surface on which the source and drain junctions are to be formed (Figure (g)).

(h) The entire silicon surface is then doped with high concentration of impurities, either through

diffusion or ion implantation (in this case with donor atoms to produce n-type doping). Diffusion is achieved by heating the wafer to a high temperature and passing the gas containing desired impurities over the surface. Figure (h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two n-type regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity.

(i) Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide, as shown in Figure (i) & (j) The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions, as illustrated in Figure (j).



Figur abrication Process of NMOS Device

B. Draw and explain operation of SRAM read and write circuitry in detail.

(Explanation =5 Marks and Diagrams = 5 Marks)

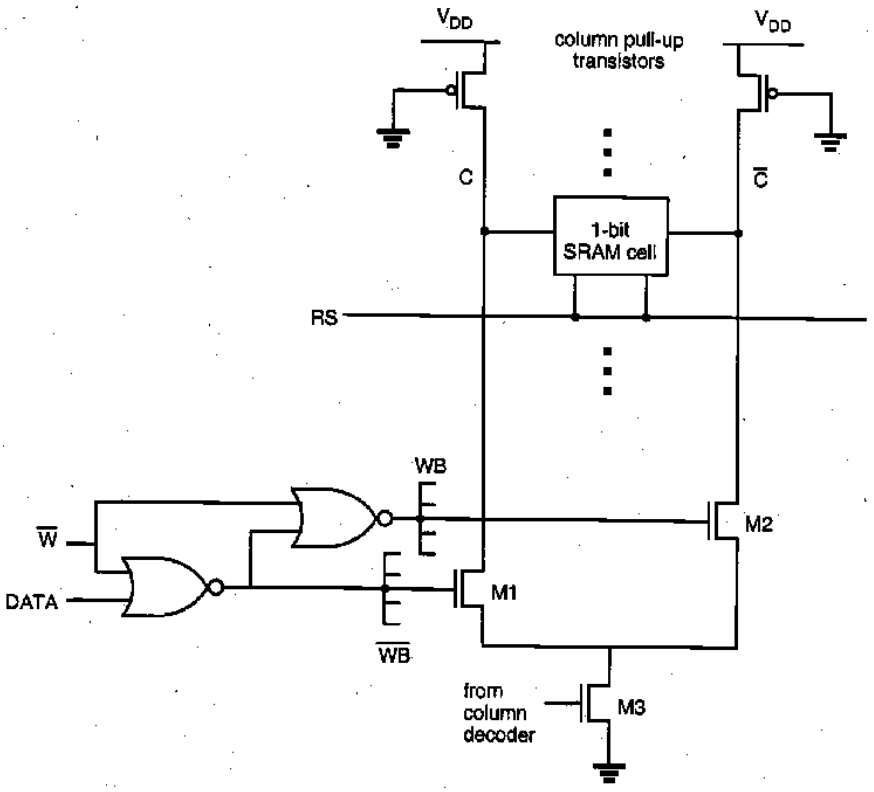
SRAM Write Circuitry

As already discussed in the preceding section, a "write" operation is performed by forcing the voltage level of either column (bit line) to a logic-low level. To accomplish this task, a low-resistance, conducting path must be provided from each column to the ground, which can be selectively activated by the data-write signals. A simplified view of the SRAM "write" circuitry designed for this operation is shown in Fig. 10.28. Here, the nMOS transistors Ml and M2 are used to pull down the two column voltages, while the transistor M3 completes the conducting path to ground. Note that M3 is driven by the column address decoder circuitry, i.e., M3 turns on only when the corresponding column address is selected. The column pull-down transistors, on the other hand, are driven by two pseudo-complementary control signals, WB and WB. The "write-enable" signal W (active low) and the data to be written *(DATA)* are used to generate the control signals, as shown in the table in Fig. 10.28. The nMOS pull-down transistors MI and M2, as well as the column selection transistor M3 must have sufficiently large ***(WIL)*** ratios so that the column voltages can

be forced to almost 0 V level during a "write" operation. Also note that the data input circuitry consisting of two NOR2 gates can be shared by several columns, assuming that one column is activated, i.e., selected by the column address decoder, at any given time.

SRAM Read Circuitry

During the "data read" operation in the SRAM array, the voltage level on either one of the columns drops slightly after the pass transistors are turned on by the row address decoder circuit. In order to reduce the read access time, the "read" circuitry must detect a very small voltage difference between the two complementary columns, and amplify this difference to produce a valid logic output level.



$\overline{W}$	*DATA*	*WB*	$\overline{WB}$	*Operation*
0	1	1	0	M1 is off, M2 is on → $V_{\overline{C}}$ low
0	0	0	1	M1 is on, M2 is off → V_C low
1	*X*	0	0	M1 and M2 are off → both columns remain high

Figure 10.28. Data write circuitry associated with one column-pair in an SRAM array.

C. What are the various regions of operation of MOSFET? Explain in detail. (10 Marks)

(Explanation of each region with suitable diagrams = 3 Marks each and Enlisting of regions = 1 Mark)

There are mainly three regions of operation in MOSFET:

- The cut-off region (Explanation in detail + Suitable diagrams = 3 Marks)
- The triode region (Explanation in detail + Suitable diagrams = 3 Marks)
- The saturation region (Explanation in detail + Suitable diagrams = 3 Marks)

Here, the cut-off region and the triode region are used to operate as a switch, and the saturation region is used to operate as an amplifier.

Q3 (20 Marks Each)	**Solve any Two Questions out of Three** **10 marks each**
A	*Compare RTL (Register Transfer Level) design and Sequential logic design.*
B	*Explain CMOS fabrication in detail with all suitable diagrams.*
C	*Explain in detail different modes of operation of MOSFET under external bias condition.*

A. Compare RTL (Register Transfer Level) design and Sequential logic design.

(Explanation = 6 Marks, Diagrams = 2 Marks and comparison = 2 Marks)

In the RTL Design methodology different types of registers such as Counters, Shift Register, SIPO (Serial In Parallel Out), PISO (Parallel In Serial Out) are used as the basic building blocks for any Sequential Logic Circuits.
On the other hand Synchronous Sequential Logic Design methodology different logic gates and different memory elements such as flip flops (to store the state of circuit at any time) is used as the basic building blocks for sequential logic circuits.
The Synchronous Sequential Logic Design Process using state diagram and its shortcomings are explained in the following example:

Lets say, we are to design a 2-bit synchronous Binary Up Counter whose count sequence is:

00 -> 01 -> 10 -> 11 -> 00 -> 01 -> ..... so on.

Step-1: In the 1st step we draw a State Diagram representing the above sequential circuit.

The State Diagram representing the above counter is shown below:

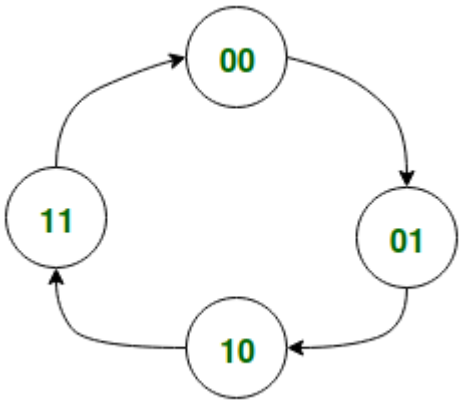


Figure – State Diagram for 2-bit UP Counter

Step-2: In the next step we derive the State Table from the above given State Diagram
The State Table is as given below:

Present State Q(n)	Next State Q(n+1)	Output
00	01	01
01	10	10
10	11	11
11	00	00

Step-3: In the third step we need to choose the type of flip flop we will be using to store the state of the circuit, for simplicity, we will be considering the Positive Edge Triggered D-type Flip-Flop. We also need to determine the number of Flip-Flops required to represent the internal state of the circuit. The general formula for the number of Flip-Flops required:
Total Number of Flip-Flops = \lceil log_2 N \rceil
Where, N = Total Number of States in State Table
Then we need to note down the Excitation Table for chosen Flip-Flop. The Excitation Table for the D-type Flip-Flop is shown below:

Present State Q(n)	Next State Q(n+1)	D
X	0	0
X	1	1

Step-4: In this step we combine the State Table from the 2nd step with the excitation table of the previous step as follows:

Q_A (n)	Q_B (n)	Q_A (n+1)	Q_B (n+1)	D_A	D_B
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

Step-5: Next, from the above table we try to express D_A, D_B as boolean functions of Q_A (n), Q_B (n).
In this case the expression for both D_A, D_B are trivial.

D_A = Q_A \oplus Q_B \hspace{2.5cm} D_B = \overline Q_B

The Final Sequential Circuit is shown below:

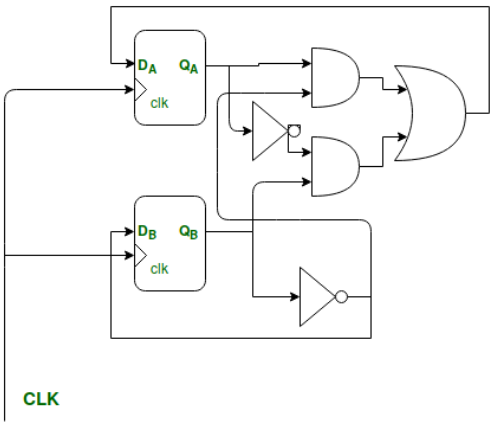


Figure – The Final Circuit

Shortcomings of the above process:

From the above example we observe that the Synchronous Sequential Logic Design process is a fairly involved process and requires us to go through a sequence of well-defined steps even for simple circuits like the one above.

Secondly, if the number of states become large then this process becomes cumbersome and time-consuming, and sometimes even impossible.
To Address the above drawbacks of the Sequential Logic Design process and to enable Digital Designers to design circuits of higher complexity with ease, the RTL design methodology was introduced. The most popular example of RTL Design is that of a Processor, which is nothing but a very sophisticated Finite State Machine with a very large number of states.

The main differences between RTL Design and Sequential Logic Design are summarized below:

RTL Design VS Sequential Logic Design

1. In RTL Design the basic building blocks are registers, Multiplexers, Adders. In Sequential Logic Design the basic building blocks are the Logic Gates, Flip-Flops.
2. RTL Design is much closer to the Behavioral Design of a Logic Circuit as it models the data flow among different registers, and hence is much more intuitive. Sequential Logic Design process is more mechanical in nature as compared to RTL design process
3. Finally, RTL Modelling allows us to synthesize complex circuits with a large number of States with much more ease as compared to Sequential Logic Design. The Sequential Logic Design techniques are only applicable to circuits having a small number of states.

B. Explain CMOS fabrication in detail with all suitable diagrams.

(Explanation =5 Marks and Diagrams = 5 Marks)

CMOS FABRICATION:
CMOS fabrication can be accomplished using either of the three technologies:

- N-well technologies/P-well technologies
- Twin well technology
- Silicon On Insulator (SOI)

The fabrication of CMOS can be done by following the below shown twenty steps, by which CMOS
can be obtained by integrating both the NMOS and PMOS transistors on the same chip substrate. For

integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs
are required in which semiconductor type and substrate type are opposite to each other.

A P-well has to be created on a N-substrate or N-well has to be created on a P-substrate. In this
article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is
fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.
The fabrication process involves twenty steps, which are as follows:
N-Well Process
Step1: Substrate
Primarily, start the process with a P-substrate.

Step 2: Oxidation

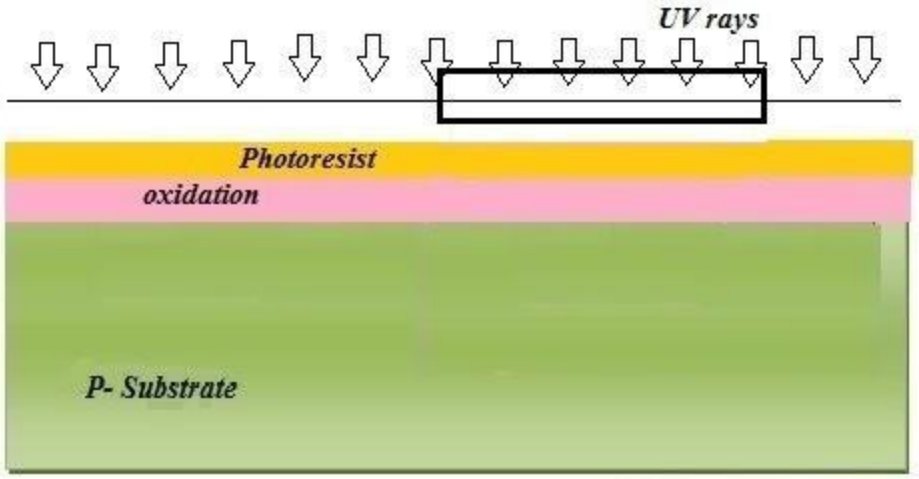
The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.

Step 3: Photoresist

A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer, is formed.

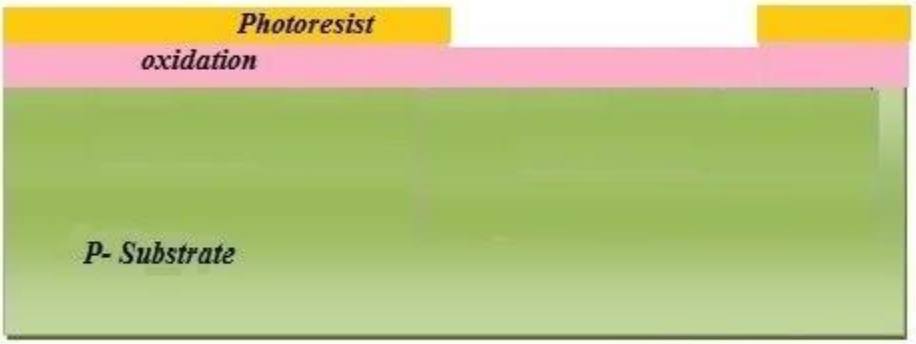
Step 4: Masking:

This step is the continuation of the photolithography process. In this step, a desired pattern of openness is made using a stencil. This stencil is used as a mask over the photoresist. The substrate is now exposed to UV rays the photoresist present under the exposed regions of mask gets polymerized.



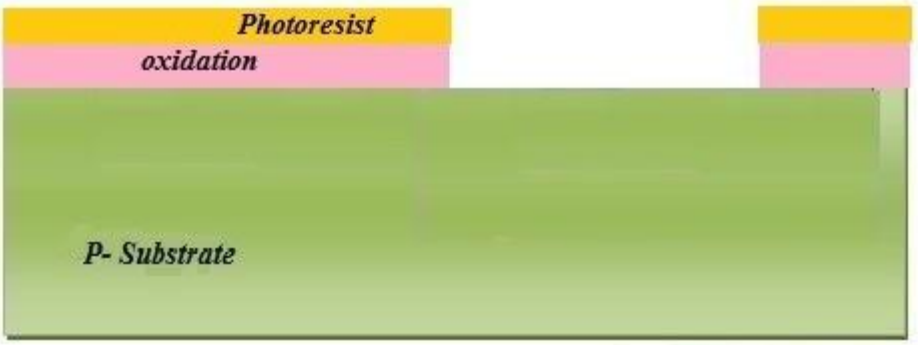
Step 5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.



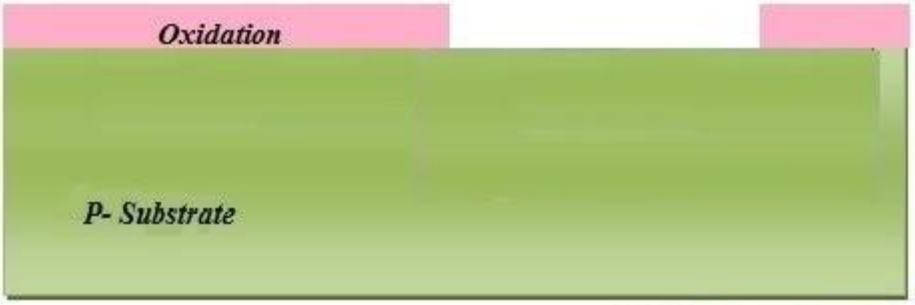
Step 6: Removal of SiO2 using acid etching

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.



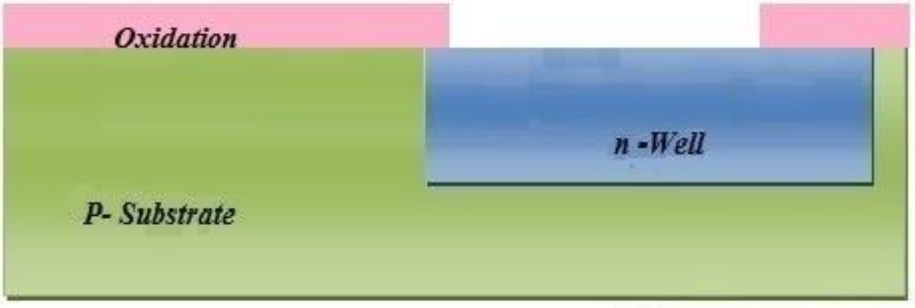
Step 7: Removal of photoresist

The entire photoresist layer is stripped off, as shown in the below figure.



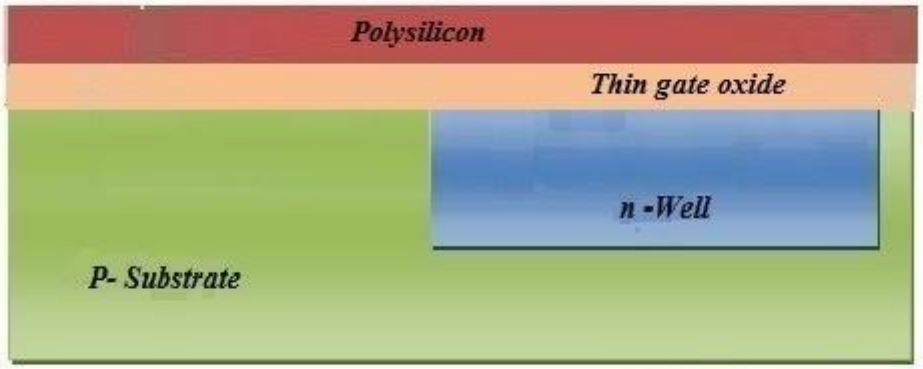
Step 8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.



Step 9: Removal of SiO2
Using the hydrofluoric acid, the remaining SiO2 is removed.

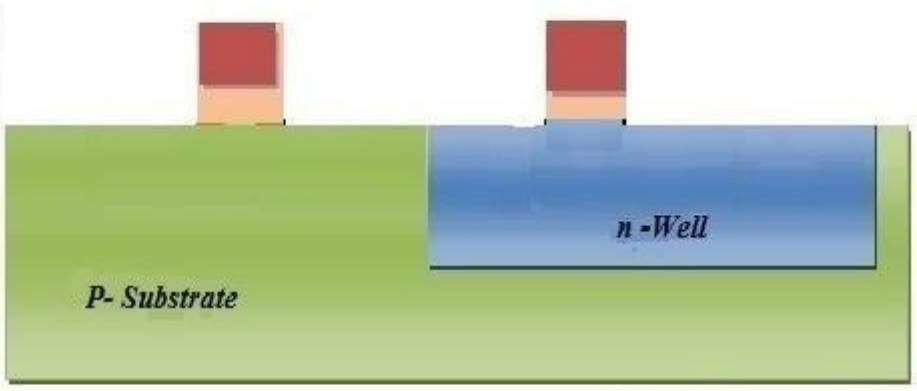
Step 10: Deposition of polysilicon
The misalignment of the gate of a CMOS transistor would lead to the unwanted capacitance which could harm circuit. So, to prevent this "Self-aligned gate process" is preferred where gate regions are formed before the formation of source and drain using ion implantation.



Polysilicon is used for formation of the gate because it can withstand the high temperature greater than 80000c when a wafer is subjected to annealing methods for formation of source and drain. Polysilicon is deposited by using Chemical Deposition Process over a thin layer of gate oxide.

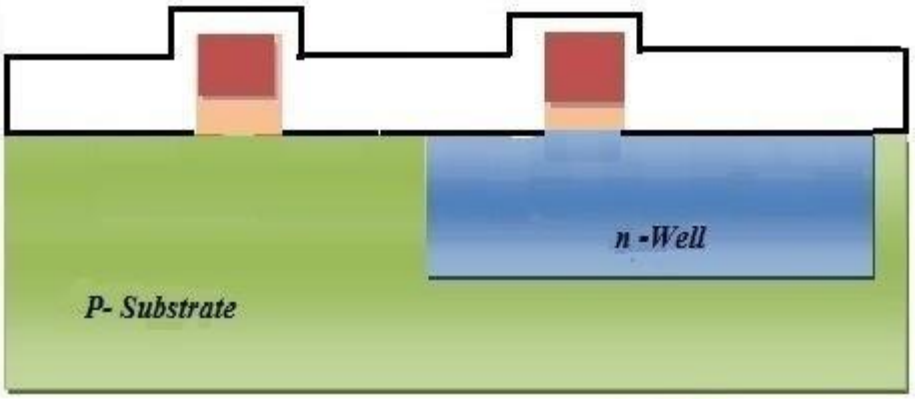
This thin gate oxide under the Polysilicon layer prevents further doping under the gate region.

Step 11: Removing the layer barring a small area for the Gates
Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



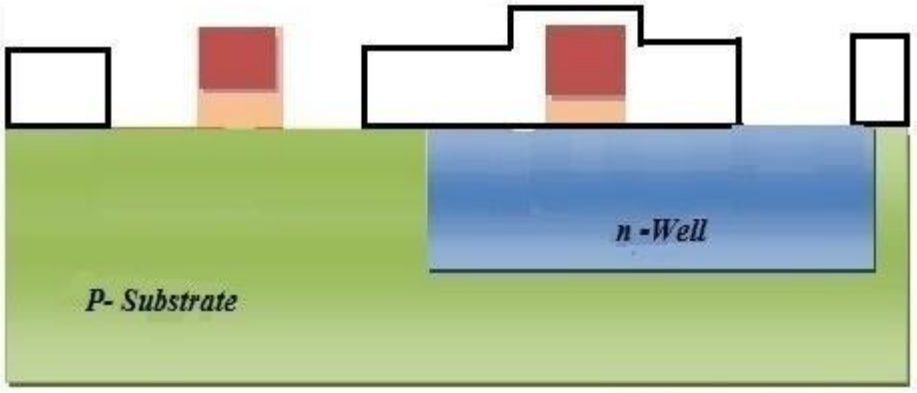
Step 12: Oxidation process

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.

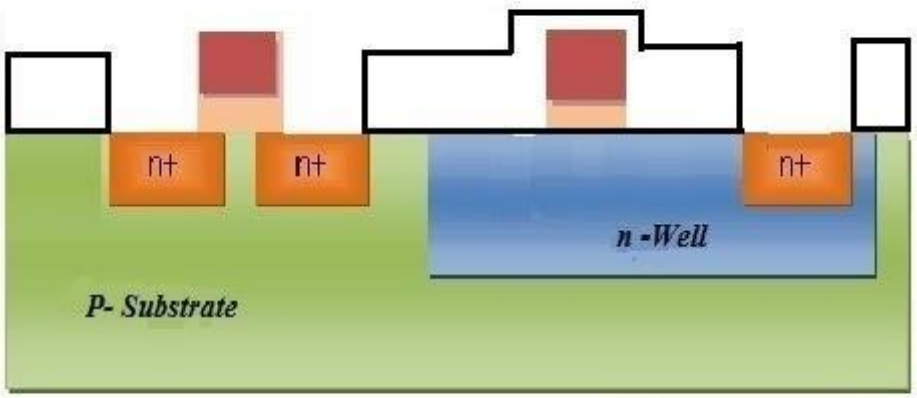


Step 13: Masking and N-diffusion

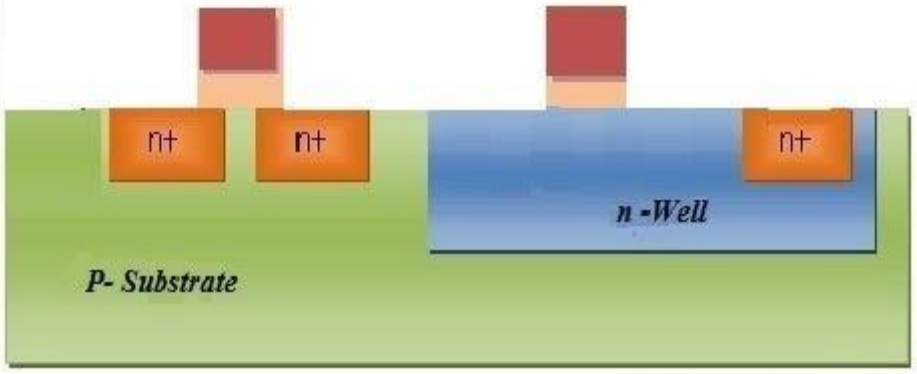
By using the masking process small gaps are made for the purpose of N-diffusion.



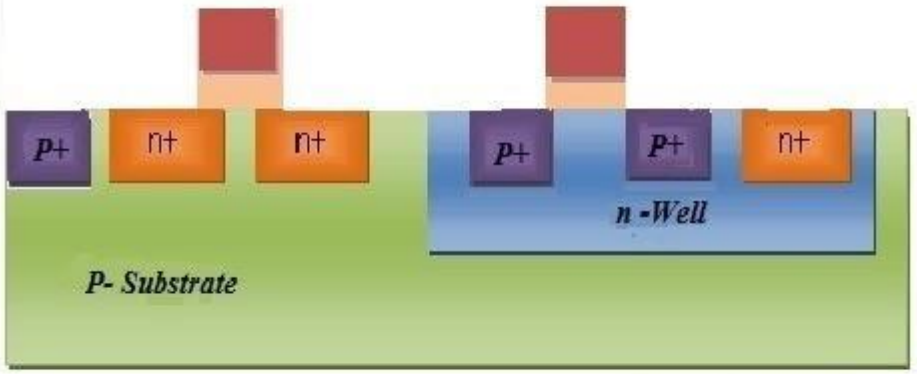
The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.



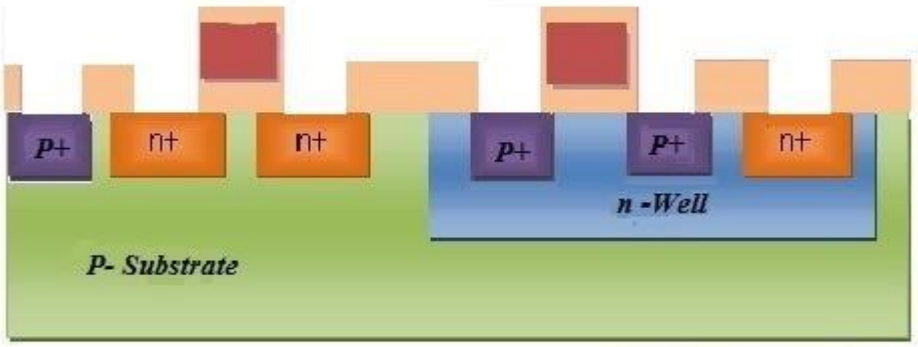
Step 14: Oxide stripping
The remaining oxidation layer is stripped off.



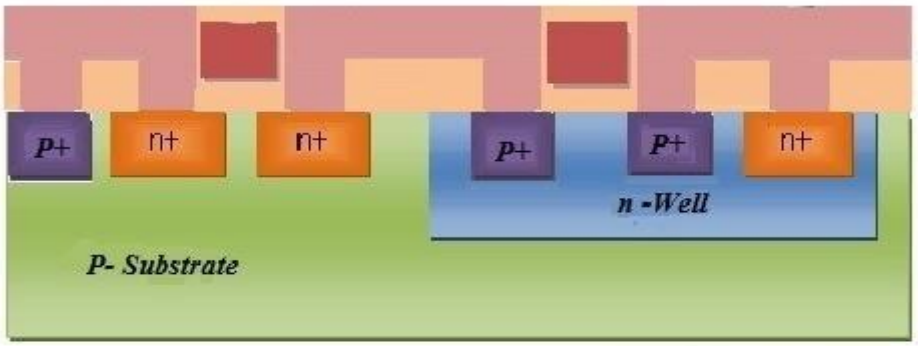
Step 15: P-diffusion
Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



Step 16: Thick field oxide
A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.

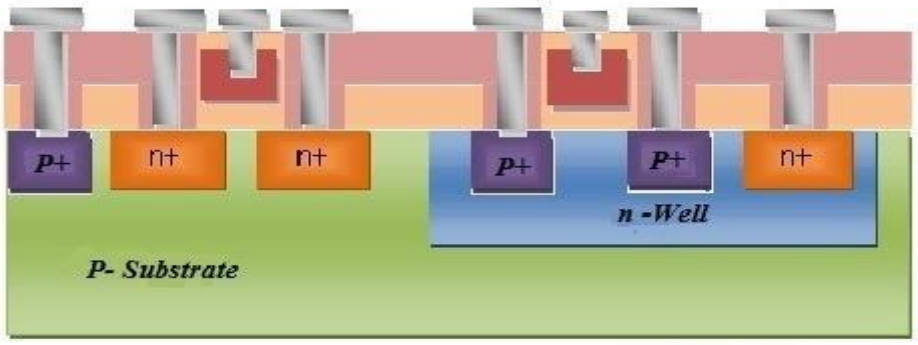


Step 17: Metallization: This step is used for the formation of metal terminals which can provide interconnections. Aluminum is spread on the whole wafer.

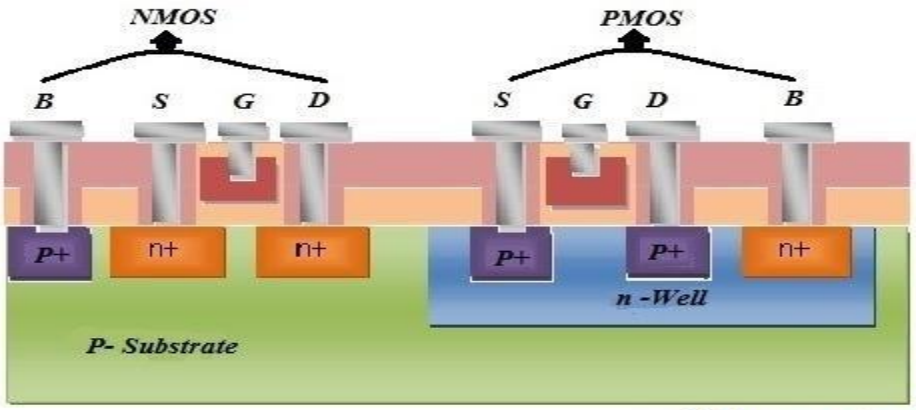


Step 18: Removal of Excess Metal: The excess metal is removed from the wafer.

Step 19: Formation of Terminals: In the gaps formed after removal of excess metal terminals are formed for the interconnections.



Step 20: Assigning the Terminal Names: Names are assigned to the terminals of NMOS and PMOS transistors.



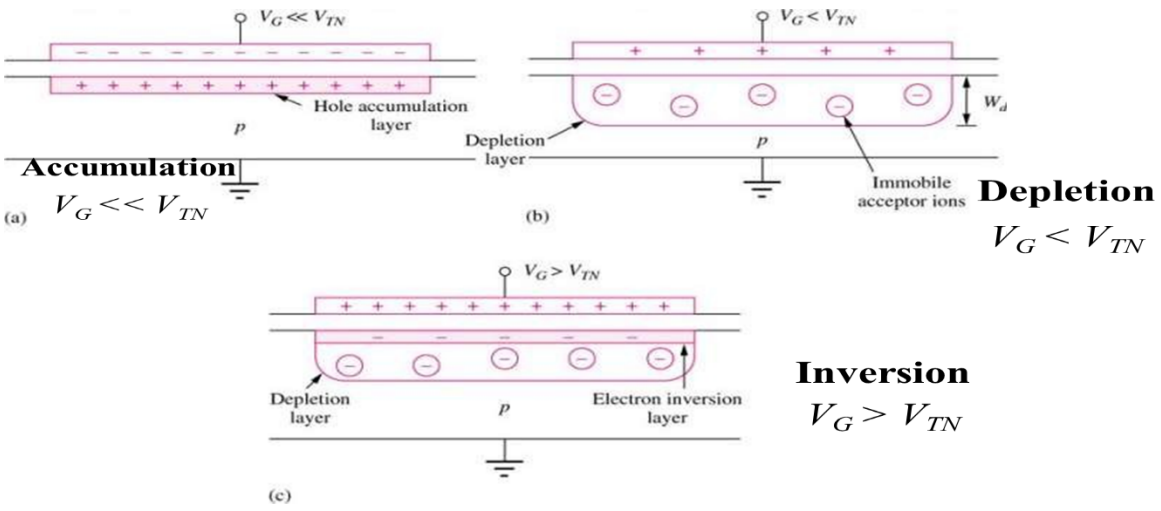
C. Explain in detail different modes of operation of MOSFET under external bias condition.

(Explanation =5 Marks and Diagrams = 5 Marks)

Assume that the substrate voltage is set at $V_B = 0$, and let the gate voltage be the controlling parameter.

Depending on the polarity and the magnitude of V_G regions can be observed for the MOS system:

- Accumulation
- Depletion
- Inversion



- Accumulation:

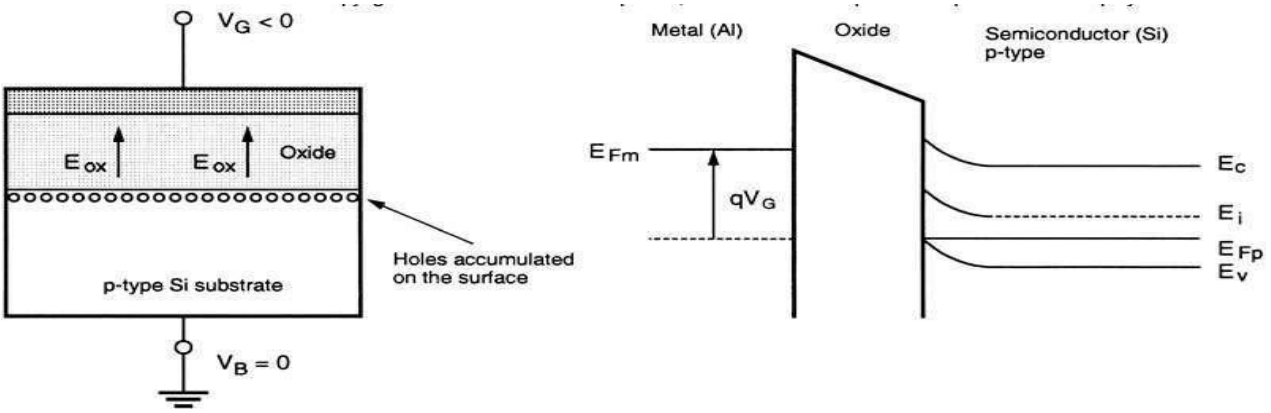
  If a negative voltage V_G is applied to the gate electrode, the holes in the p-type substrate are attracted to the semiconductor-oxide interface.

  The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier accumulation on the surface.

  Note that in this case, the oxide electric field is directed towards the gate electrode.

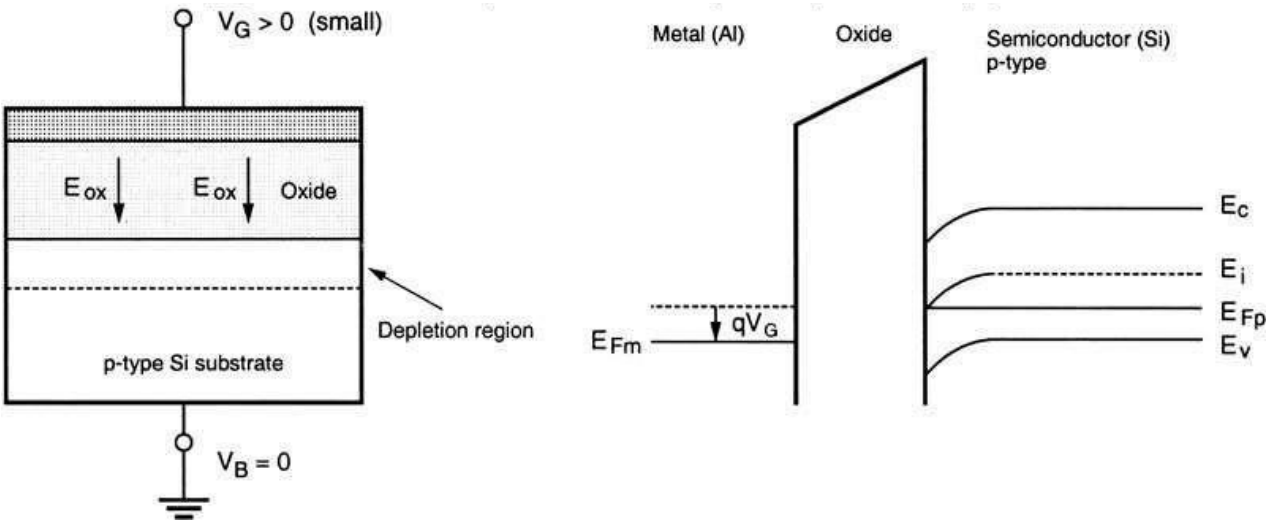
The negative surface potential also causes the energy bands to bend upward near the surface.
While the hole density near the surface increases as a result of the applied negative gate bias, the electron (minority carrier) concentration decreases as the negatively charged electrons are pushed deeper into the substrate.

The MOS System under External Bias (Accumulation)



- Depletion:

  A small positive gate bias V_G is applied to the gate electrode.
  Since the substrate bias is zero, the oxide electric field will be directed towards the substrate in this case.
  The positive surface potential causes the energy bands to bend downward near the surface.
  The majority carriers, i.e., the holes in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes will leave negatively charged fixed acceptor ions behind.
  Thus, a depletion region is created near the surface.
  Under this bias condition, the region near the semiconductor-oxide interface is nearly devoid of all mobile carriers.



- Inversion:

  If the positive gate bias is further increased i.e., $V_G > 0$ (Large)

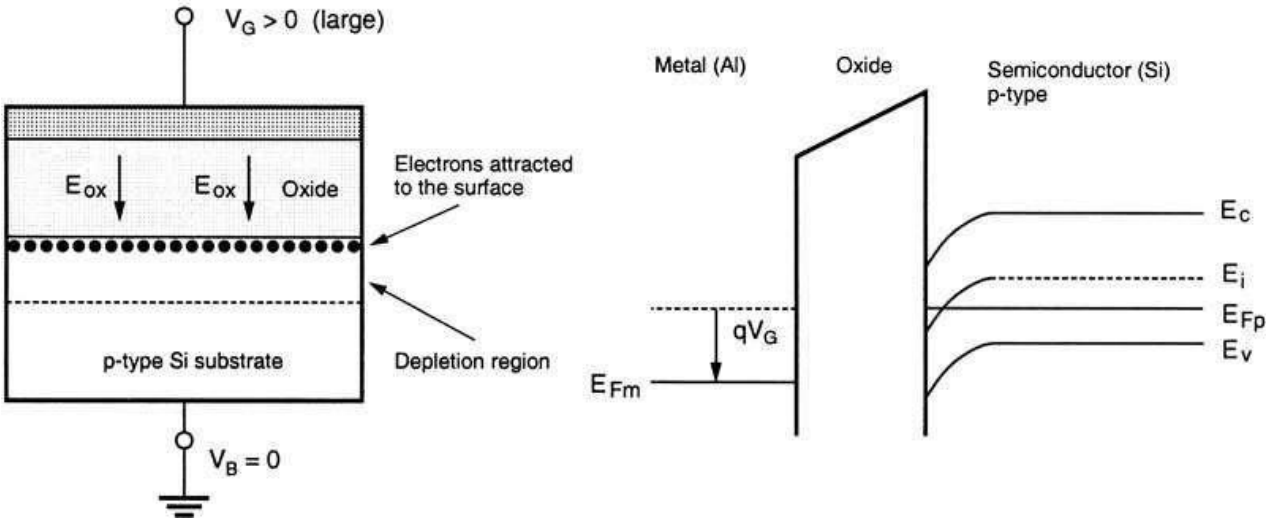
  As a result of the increasing surface potential, the downward bending of the energy bands will increase as well.

  Eventually, the mid-gap energy level E_i becomes smaller than the Fermi level E_{PF} on the surface, which means that the substrate semiconductor in this region becomes n-type.

  Within this thin layer, the electron density is larger than the majority hole density, since the positive gate potential attracts additional minority carriers (electrons) from the bulk substrate to the surface.

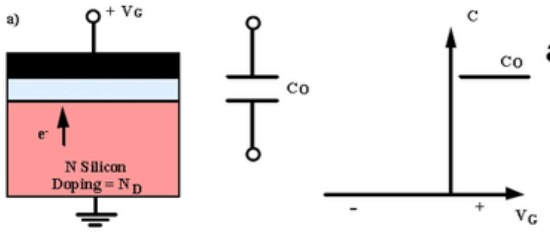
  The n-type region created near the surface by the positive gate bias is called the inversion layer, and this condition is called surface inversion.

  It will be seen that the thin inversion layer on the surface with a large mobile electron concentration can be utilized for conducting current between two terminals of the MOS transistor.



- **DC bias + small AC high frequency signal applied.**

$$C = \frac{dQ}{dV}$$

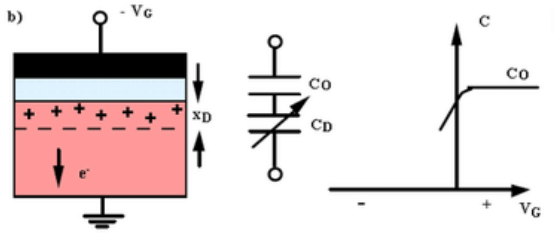


a) Accumulation majority carrier drawn to surface

$$C_{ox} = \frac{\varepsilon_{ox} \cdot A}{x_{ox}}$$

Charge Density

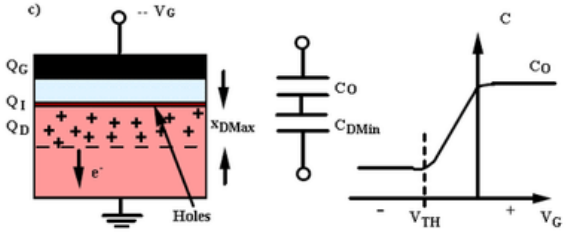
$$|Q_G| = |Q_D| = N_D x_D$$



b) Depletion minority carrier drawn to surface majority carriers repelled

$$C_D = \frac{\varepsilon_{Si} \cdot A}{x_D}$$

$$|Q_G| = N_D x_D + Q_I$$



c) Inversion minority carrier layer exists

Q4. (20 Marks Each)		
A	**Solve any Two**	**5 marks each**

i.	*Implement the equation X = ((A + B) (C + D + E) + F) G using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?*
ii.	*Compute the following for the pseudo-NMOS inverter shown in Figure:* *a. VOL and VOH* *b. NML and NMH* *c. For an output load of 1 pF, calculate tp_{LH}, tp_{HL}, and tp are the rising and falling delays equal? Why or why not?*
iii.	*Suppose we want to implement two logic functions given by F=A+B+C and G=A+B+C+D. Assume both true and complementary signals are available.* *a) Implement these functions in dynamic CMOS as cascaded stages so as to minimize the total transistor count.* *b) Discuss any conditions under which this implementation would fail to operate properly.* *c) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b)?*
B	**Solve any One** **10 mark each**
i.	*Explain stick diagram rules with color coding and draw a stick diagram for CMOS inverter.*
ii.	*Discuss about Lambda design rules in detail.*

A. (i) Implement the equation X = ((A + B) (C + D + E) + F) G using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

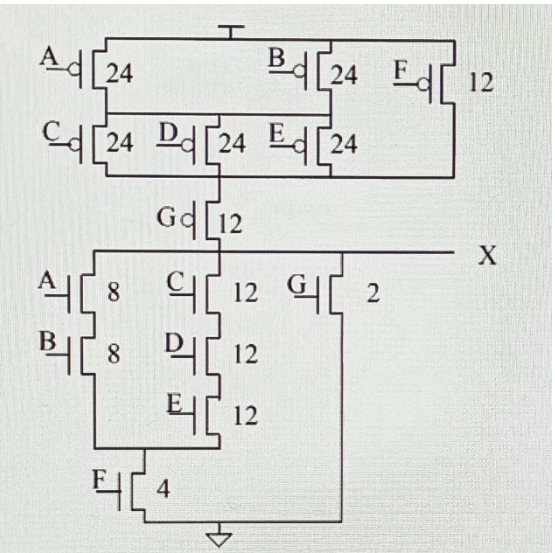
(Explanation = 03 Marks and Diagram = 02 Marks)

Solution

Rewriting the output expression in the form

$$X = ((A + B) (C + D + E) + F) G = ((AB + CDE) F) + G$$

allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.



The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS W/L=2 and PMOS W/L=6.

The worst-case pull-up resistance occurs whenever a single path exists from the output node to V_{dd}. Examples of vectors for the worst case are ABCDEFG=1111100 and 0101110.

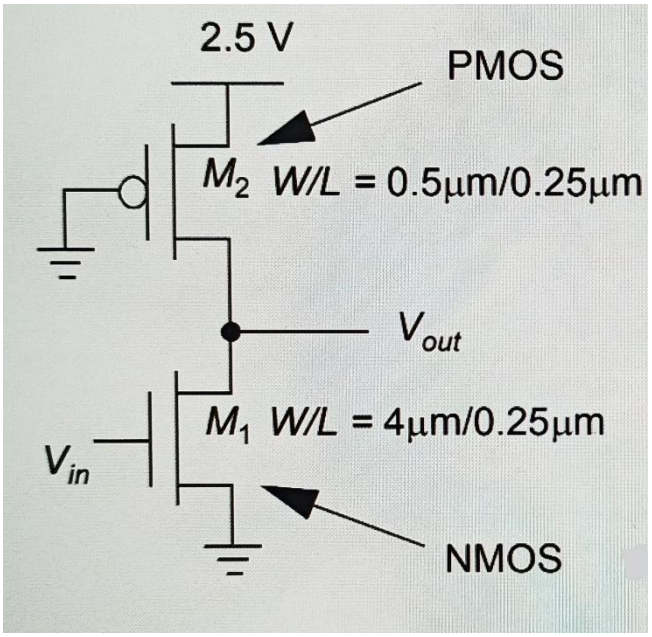
The best-case pull-up resistance occurs when ABCDEFG=0000000.

The worst-case pull-down resistance occurs whenever a single path exists from the output node to GND. Examples of vectors for the worst case are ABCDEFG=0000001 and 0011110.

The best-case pull-down resistance occurs when ABCDEFG=1111111.

A.(ii) Compute the following for the pseudo-NMOS inverter shown in Figure:

a. V_{OL} and V_{OH}
b. N_{ML} and N_{MH}
c. For an output load of 1 pF, calculate tp_{LH}, tp_{HL}, and tp are the rising and falling delays equal? Why or why not?



(a = 02 Marks, b = 01 Mark and c = 02 Marks)

a. V_{OL} and V_{OH}

Solution

To find V_{OH}, set Vin to 0, because V_{OL} is likely to be below VT0 for the NMOS. If Vin=0, then M1 is off, so the PMOS pulls the output all the way to the rail. So,

$$V_{OH}=V_{DD}=2.5V.$$

To find V_{OL}, set Vin = V_{OH} = 2.5V. The NMOS is all the way on, but so is the PMOS.

To find V_{OL}, we can write a current balancing equation at the output node:

$$I_{DP}+I_{DN}=0.$$ First,

we must determine the region of operation for each device. We can assume that $V_{DS} = V_{OL}$

for the NMOS is less than V_{DSAT}, so the NMOS is in the linear region. V_{DS} for the PMOS will

be more negative than V_{DSAT}, and V_GTp = -2.1, so the PMOS is velocity saturated. The equation is therefore:

Plugging in numbers (process parameters such as V_{DSAT} appear in tables in previous chapters) gives:

$$-30 \cdot 2 \cdot -1 \cdot (-1.6) \cdot (1 - 0.1(V_o - 2.5)) + 115(16) \cdot V_o \cdot (2.07 - 0.5V_o) \cdot (1 + 0.06V_o) = 0$$

Solving for Vo gives V_{OL} = 31.6mV.

b. N_{ML} and N_{MH}

Solution

Rather than calculating the derivative of the current, we will estimate V_{IL} and V_{IH} from the simulated V_{TC}. This approach estimates that the noise margin low is about 0.47Vand the noise margin high is about 1.67V.

c. For an output load of 1 pF, calculate tp_{LH}, tp_{HL}, and tp are the rising and falling delays equal? Why or why not?

The average current for the HL transition through the PMOS is

$0.5(I_{VDD=2.5} + I_{VDD=1.25})$. $I_{(VDD=2.5)} = 0$.

$I_{(VDD=1.25)} = -30(2)(-1)(-2.1+0.5) *(1+0.1(1.25)) = 108\mu A$.

Thus, I_{avg} for the PMOS is 54µA.

For the NMOS,

$I_{(VDD=2.5)} = 115(16)(0.63)(2.07-.63/2)(1+0.06*2.5)=2.4mA$ and

$I_{(VDD=1.25)} = 115\ (16)\ (0.63) *(2.07-.63/2)(1+0.06*1.25) = 2.2mA$.

So, I_{avg} for the NMOS is 2.3mA.

The average current discharging the capacitor is then 2.3mA-54uA = 2.25mA.

Then $tp_{HL} = C*\Delta V/I_{avg} = 556ps$.

For tp_{LH}, the NMOS is off, so we can use equivalent resistance to find the transition time. From the table of resistances in the text, we can calculate REQ = 31k /(W/Lp) =15.5k . Then $tp_{LH} = 0.69*C*R_{EQ}$. So tp_{LH} = 10.7ns.

$Tp = (tp_{LH} + tp_{HL})/2$ = 5.6ns. The rising delay is much longer because the PMOS is very weak relative to the NMOS.

A.(iii) Suppose we want to implement two logic functions given by F=A+B+C and G=A+B+C+D. Assume both true and complementary signals are available.

a) Implement these functions in dynamic CMOS as cascaded Ø stages so as to minimize the total transistor count.

b) Discuss any conditions under which this implementation would fail to operate properly.

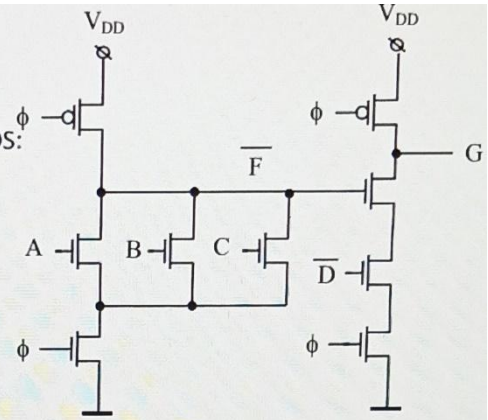
c) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b)?

(a = 02 Marks, b = 01 Mark and c = 02 Marks)

Solution:

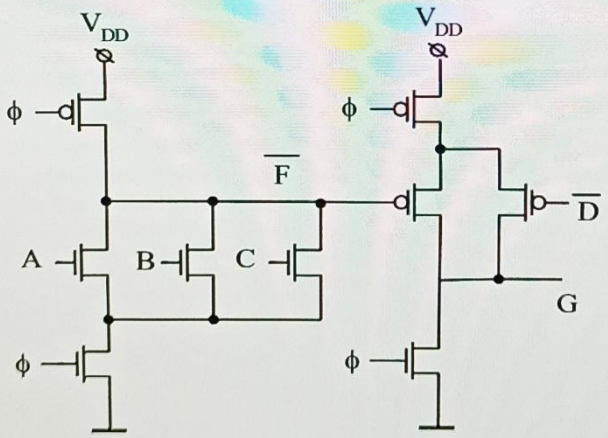
a. Implementation of the functions in simple dynamic CMOS:

$$G = \overline{\overline{F}\,\overline{D}} = A + B + C + D$$



b. This circuit will fail to operate. When A+B+C=1, $\overline{F}$ will make a transition 1->0, which cannot be applied directly to the second stage. If D=0 for example, G will be discharged at the beginning of the evaluation phase. Therefore G will have an incorrect value (0) for this combination of input signals.

c. To ensure operation, we can use an np-CMOS implementation. The stages in np-CMOS can be cascaded directly since every stage produces the correct signal transition for the opposite type of logic connected to its output.



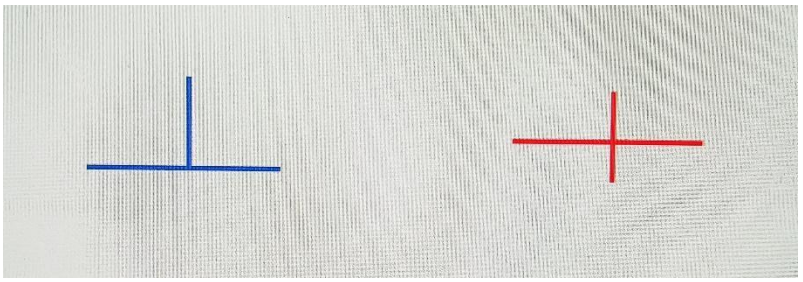
B.(i) Explain stick diagram rules with color coding and draw a stick diagram for CMOS inverter.

(Explanation =5 Marks and Diagrams = 5 Marks)

Stick Diagrams – Some Rules

Rule 1:

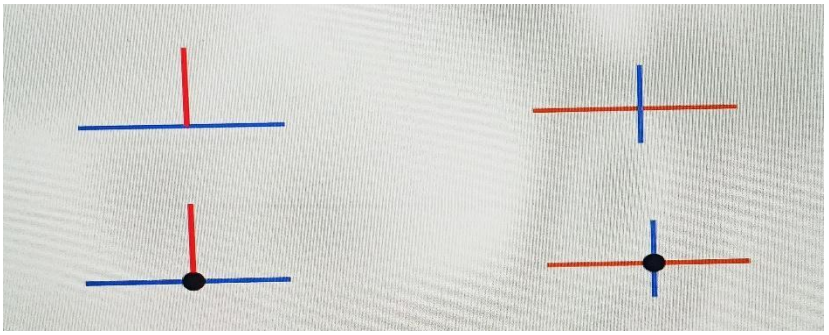
When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.



Rule 2:

When two or more „sticks" of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed, we have to show the connection explicitly)

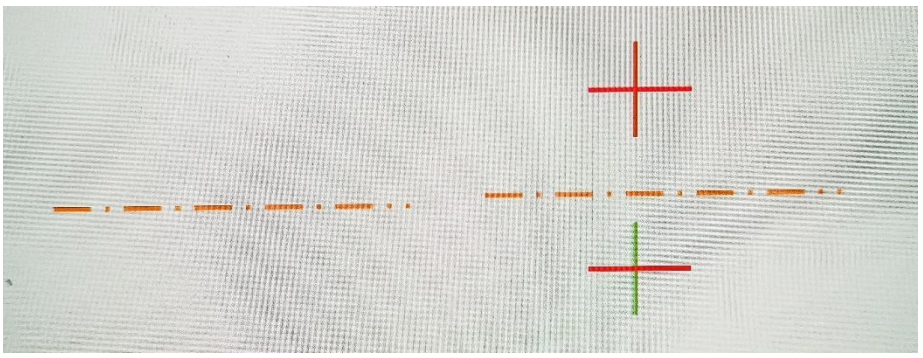


Rule 3:

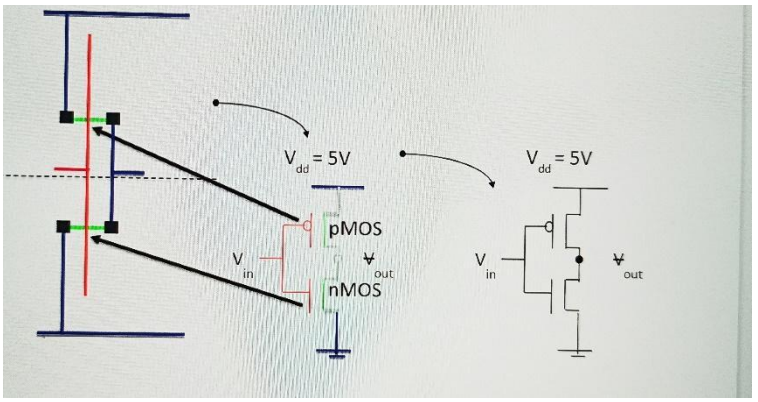
When a poly crosses diffusion it represents a transistor.

Rule 4:

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.



CMOS Inverter Stick Diagram



B.(ii) Discuss about Lambda design rules in detail.

(Explanation =5 Marks and Diagrams = 5 Marks)

- Lambda-based (scalable CMOS) design rules define scalable rules based on λ (which is half of the minimum channel length)
- Stick diagram is a draft of real layout, it serves as an abstract view between the schematic and layout.
- Circuit designer in general want tighter, smaller layouts for improved performance and decreased silicon area.
- On the other hand, the process engineer wants design rules that result in a controllable and reproducible process.
- Generally, we find there has to be a compromise for a competitive circuit to be produced at a reasonable cost.
- All widths, spacing, and distances are written in the form
- λ = 0.5 X minimum drawn transistor length
- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits

- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

DESIGN RULES

- Minimum width of PolySi and diffusion line 2λ
- Minimum width of Metal line 3λ as metal lines run over a more uneven surface than other conducting layers to ensure their continuity
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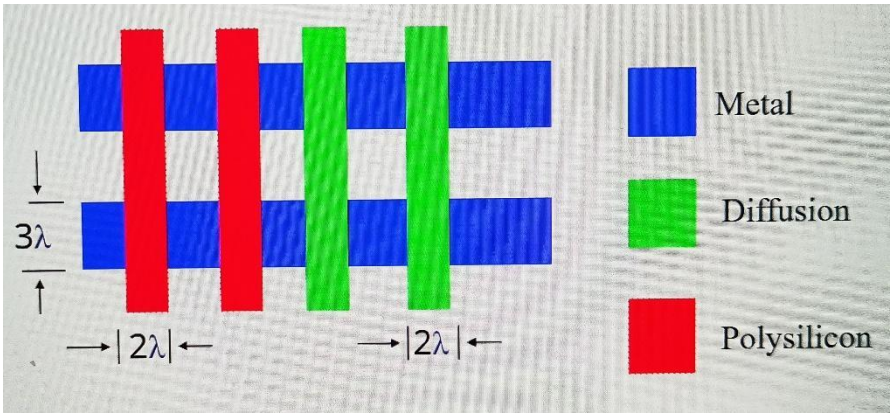

- PolySi – PolySi space 2λ
- Metal - Metal space 2λ
- Diffusion – Diffusion space 3λ To avoid the possibility of their associated regions overlapping and conducting current
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