Vidya Vikas Education Trust's
Universal College of Engineering
Approved by AICTE, DTE, Maharashtra State Goverment and Affiliated to Mumbai University
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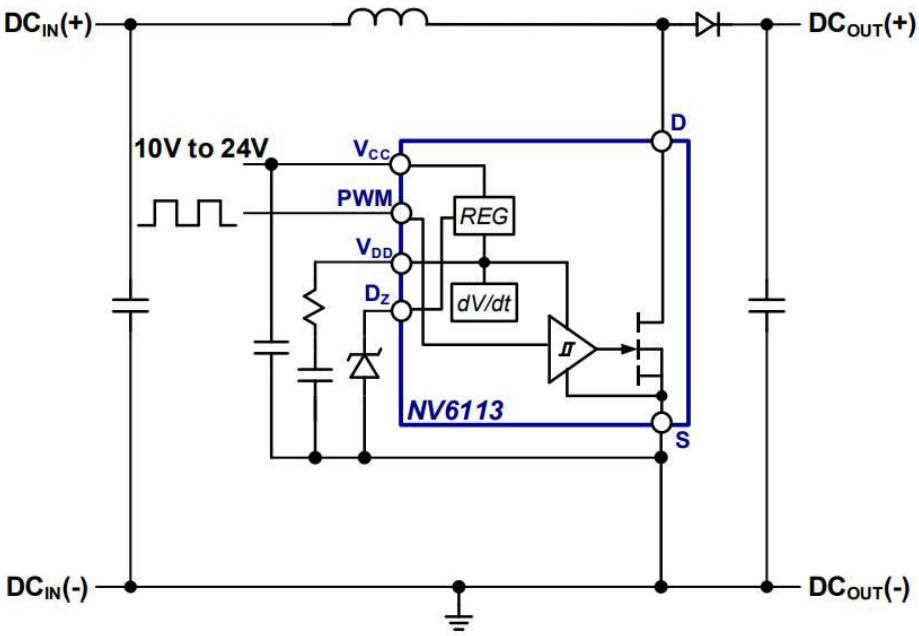
Department Vision:

To be recognized for practicing the best teaching-learning methods to create highly competent, resourceful and self-motivated young electronics engineers for benefit of society.

Department Mission:

- To nurture engineers who can serve needs of society using new and innovative techniques in electronics.
- To improve and apply knowledge of electronics subjects through participation in different technical events.
- To enhance carrier opportunities of electronic students through industry interactions and in plant training.
- To install the passion and spirit among students to pursue higher education in electronics and entrepreneurship.

GaN IC handles 500W for consumer PSUs



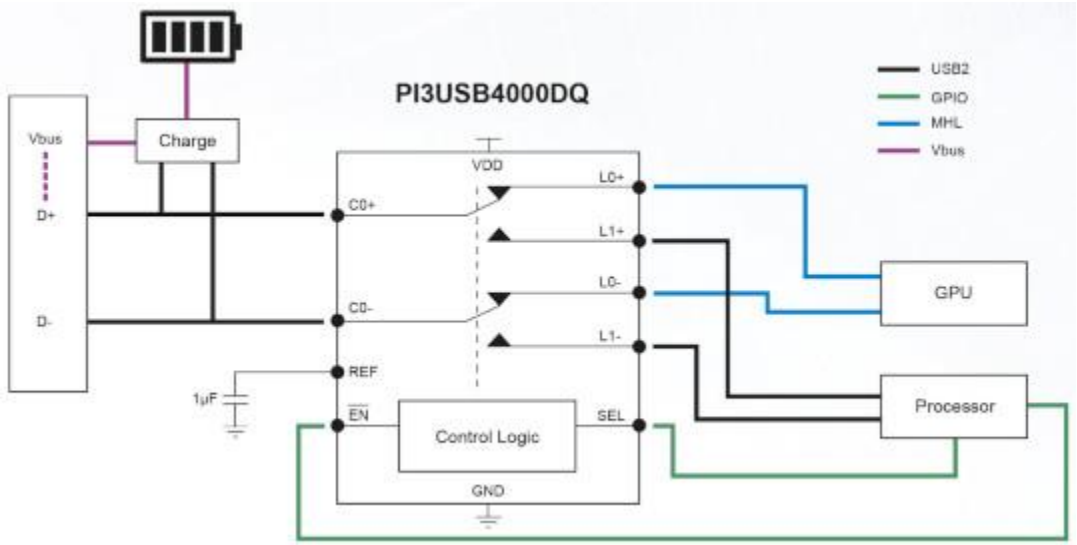
"With the higher-power NV6128, we extended the effective power range to 500W for the consumer market and look beyond that to multi-kW data centre, e-mobility and new energy applications," said company CEO and founder Gene Sheridan. According to Navitas CTO Dan Kinzer, switching at 200kHz in a "modern high-speed totem-pole" architecture, the device can yield a complete 300W PSU at >1.1W/cm^3. "When you crank up the speed to MHz+, you get another major step-increase in power density," he said.

The chip runs from 10 to 24V and over case temperatures for -40 to 125°C. The gate driver is integrated – controlling the crucial parasitics between driver and gate. Control need to be through a separate microcontroller, DSP or other integrated circuit. For example, inside Oppo's ~80 x 40 x 10mm 50W SuperVooc charger are a pair of Navita's earlier (170mΩ) NV6115 ICs plus a TI UCC28782 active clamp fly-back controller switching at ~500 kHz and an On Semi NCP51530 level-shifter-driver.

The company refers to its products as 'monolithic' and, although not stated explicitly, the switching transistors seem to be enhancement-mode HEMTs, referred to it as 'eMode FETs'.
Although rated for 650V, NV6128 can handle <100µs non-repetitive 800V surges (from start-up or line interruption) and <100ns repetitive 800V spikes (from leakage inductance).
Packaging is 6 x 8mm PQFN package with integrated cooling pad.
200-500W applications are foreseen in all-in-one PCs, TVs, game consoles, gaming laptops and chargers for e-scooters and e-bikes. Branded 'GaNFast', Navitas power ICs have been used in fast chargers by companies including Lenovo, Dell, Oppo and Xiaomi, with over 13,000,000 parts shipped, claimed CEO Sheridan.

Source: https://www.electronicsweekly.com/news/products/power-supplies/gan-ic-handles-500w-consumer-psus-2021-05/

Automotive USB 2.0 mux/demux switches with 24V protection



- PI3USB4000DQ is a 2:1/1:2 switch for differential bi-directional DPDT
- PI3USB4002AQ is a 1:1 switch for differential bi-directional DPST switching

24Vdc withstanding is provided on one high-speed data port ('C0' pins), enabling them to tolerate shorts between D± and Vbus on both USB and USB Type-C connectors. This "protects the system from damage due to connector or cable damage", according to the company.
Co pins also get ESD protection to IEC61000-4-2 10kV.

L0, L1 and Vdd pins are only protected to 6V.

The 'Ref' pin is also 24V tolerant, and must be fitted with a capacitor rated to suit this.
Over-voltage protection is implemented at 4.75V to immediately switch off the channels when over-voltage condition is detected.
For signal integrity with USB 2.0 signals, bandwidth is 1GHz.
In both devices, typical on capacitance and resistance are 7pF and 5Ω, and propagation delay is 250ps.
Typical 240MHz off isolation and cross-talk are -30dB and -35dB respectively/
Operation is over 2.7 to 5.5V and -40°C to 125°C, and consumption is typically 35µA (PI3USB4002AQ – SPDT – switches to a 1µA low-consumption mode when the data channel is off).
Control pins support 1.8V logic.
Both come in a 1.5 x 2mm U-QFN1520-10 package and are AEC qualified in IATF 16949 certified manufacturing sites and support PPAP documentation.

Source: https://www.electronicsweekly.com/news/products/power-supplies/automotive-usb-2-0-mux-demux-switches-24v-protection-2021-05/

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Why semiconductor design is set to look very different

If 2020 propelled the semiconductor market to new levels of demand, just wait for what 2021 and beyond have in store.

Fabs are already at capacity and semiconductors can be found in more products and systems, powering everything from personal devices to self-driving vehicles. Despite the impact of the pandemic on the global economy, International Data Corporation (IDC) says that demand for semiconductors remained strong, fuelled by the growth in cloud computing and devices to support remote work and learning.

Its own research bears this out. According to IDC's Semiconductor Applications Forecaster (SAF), in 2020 worldwide semiconductor revenue grew to $442 billion, an increase of 5.4% compared to 2019. IDC has now forecast that the semiconductor market will reach $476 billion in 2021, which would mean a 7.7% year-over-year growth rate.

There are some clear trends within the industry too. For instance, PWC has predicted that the market for AI-related semiconductors will reach $30 billion by 2022, representing an AGR of almost 50%. At the same time, there is very much still a place for traditional system on chips (SoCs). Memory chips are expected to carry on holding the biggest market share through 2022, and silicon chips will dominate for the next couple of decades.

New technologies and players

Other factors shaping the future of semiconductors stem from technology directions, such as a burgeoning focus on open source hardware. As that gains momentum, it is going to change how organisations think about design, and will encourage a more collaborative and partnership approach to development.

The IoT is driving demand for more cost-effective semiconductors and on a larger scale. Similarly, 5G enables the bandwidth to finally support vast, interconnected infrastructure, for example for transportation, combining inputs from multiple API-connected sources. To achieve the scale required, standards-based reusable and sharable IP is going to be key to meet design requirements, but in a way that supports distribution and collaboration, while also meeting safety and security requirements. Open source could be a key to achieving that scale.

The nature of the players involved in the industry is shifting too, such as the introduction of vertically-integrated systems and non-traditional semiconductor firms, who may prefer to create their own devices and platforms for greater control. A good example of this being Apple's M1, a processor designed for Mac, which furthers their commitment to building key functionality internally. This adds another interesting dimension to the industry, increasing competition and sources of innovation.

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Remote collaboration

As much a necessity as a trend, semiconductor design teams have had to embrace remote collaboration on an unprecedented scale. Of course, to some extent that was already happening, but the pandemic made it a necessity for survival in many cases.

In these virtual environments, problems with workflow processes became impossible to ignore, with sharing of IP happening on a much wider scale. Addressing issues around collaboration and security has become a priority, and once organisations have achieved that, they will be equipped with experience that can be used to improve processes irrespective of location, whether in the design office or working remotely.

Regardless, the shifting nature of the semiconductor market reinforces some age-old challenges for designers: keeping pace with change and complexity, controlling costs, making sure a project stays on track and in line with requirements, and then meeting delivery deadlines. Many semiconductor product launches do not meet the original launch date. Contributing factors can include: the difficulty of collaboration across remote and dispersed teams, company acquisitions leading to design silos, not addressing management of exploding design data sizes, or keeping up with increasing complex design environments.

IP reuse versus over-sharing

IP reuse has long been talked about as the solution to keeping up with the sheer scale of developments required, avoiding unnecessary reinventing of the wheel, speeding up time-to-market and drastically reducing costs. A variety of assets can be reused include source code and binaries for software, plus hardware IP like arm processor cores.

The theory is sound, but successful management of IP reuse is another matter. Many organisations have multiple systems, including shared drives and source code management, to store and track all these files, but that makes it difficult to manage — let alone reuse — these files. Fortunately, there are a variety of tools and techniques that can help designers overcome those barriers, but those have to include a strong structure and control around reuse. While sharing of IP is the route to faster development, it can also bring risks around management and security. Traceability of IP and meta-data — who has access to what, where, and how they are using those assets — becomes critically important to the success of projects.

There is a balance required between sharing and over-sharing, which is why a combination of traceability, visibility, and access control are essential for modern semiconductor design. Of course, manual traceability is widely adopted, but to address large and complex projects, more organisations are using tools that automate much of the process, from requirements through to design and verification. This makes it easier to track which IPs have been used, where, and when, and in turn avoid costly respins in design. Changes in requirements can be surfaced and communicated earlier and more clearly. Traceability also supports better remote collaboration.

In addition, creating a ‘single source of truth’, or data management platform, can unite all the software and hardware components within a project. Even small files become simpler to locate

and reuse, and there may be millions of those within an enterprise, not just the big complex designs. A single source of truth is typically based on using a version control system, which provides real-time and historic visibility into all the assets involved, while allowing users to carry on working with their preferred tools and systems.

A single source of truth is also critical to identifying configuration issues across systems, in hardware and software, that are masked by the complexity of the systems. In turn, that makes it easier to bring together collaboration across remotely located teams, both internally and externally.

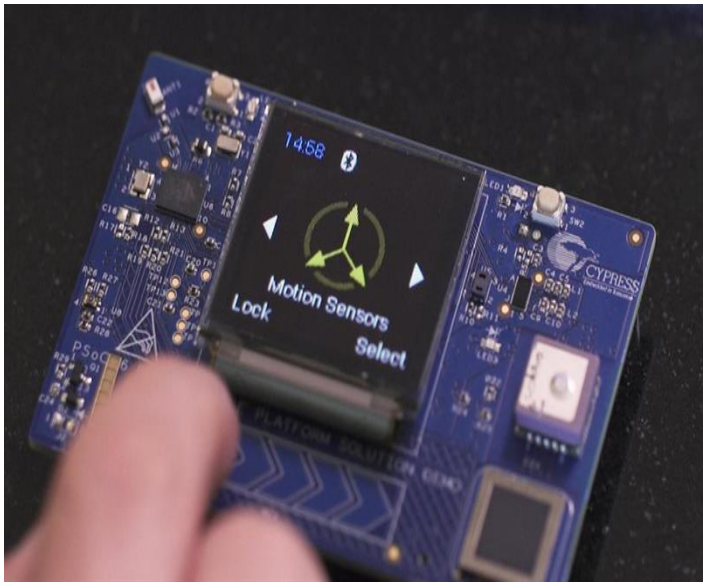
Overcoming IP leakage

With comprehensive traceability and visibility in place, then it becomes more feasible to identify and prevent IP leakage, a perennial and costly concern in the semiconductor industry. Some of the root causes include dispersed collaborators, inadequate control over who can view and download IP, and users inadvertently exporting IP to an unauthorised source. With semiconductor markets becoming ever more global, mitigating IP leakage is of paramount importance.

Semiconductor design is going through a period of unprecedented change. The events of the last year, however, have given us a blueprint of how to handle the needed changes to collaboration and culture. The good news is that there are tools available to provide the needed traceability to facilitate IP reuse at scale while also providing the security and communication layers for effective collaboration.

Source:https://www.newelectronics.co.uk/electronics-technology/why-semiconductor-design-is-set-to-look-very-different/236394/

Analogue programmability



When you look at the success of the field-programmable gate array (FPGA) in capturing a wide range of designs where flexibility counts more than volume price, the attraction to do the same for analogue makes a lot of sense. But the analogue cousin of the FPGA has faced more of a struggle.

Conceptually, the field-programmable analogue array (FPAA) is only a little younger than its logic-oriented big brother: the first proposals from researchers appeared in the late 1980s, with work at two independent groups, one at Caltech and the other at the University of Southern California. Since then the concept has been tried commercially though with mixed

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results. The most famous proponent has been Anadigm, which started as a spinout from glassmaker Pilkington mid-1990s before being acquired by Motorola and again being spun out as a company based near the semiconductor company's Arizona fabs.

For its parts Anadigm chose a switched-capacitor implementation, which was already a technique used in the design of ASICs to add analogue functions cost effectively to a predominantly digital process. Switching capacitor-based circuits on and off rapidly provides the ability to build resistor networks that are more accurate than physical CMOS resistors and useable as long as the signal bandwidth is below the switching rate. The somewhat younger start-up Okika Technologies has similarly chosen a switched-capacitor approach for tuning the parameters of on-chip amplifier modules and I/O cells that are provided alongside digital lookup tables for control.

A key issue for companies selling FPAAs is the tension between the need for small size and flexibility versus cost and performance in an environment where discrete analogue circuitry, even with highly specific functions, is plentiful and often inexpensive.

Andrea Riverso, head of product management for semiconductors at distributor Farnell, says users with a need for fast prototyping or working on research applications are likely to benefit more from programmable-analogue parts. Once a requirement becomes specific, it can be more cost-effective to develop a hardwired implementation and still be able to add some level of programmability, possibly by switching some elements in and out of the circuit.

A key question is how much in-field flexibility is needed. An FPAA can make sense if there is need to cater for different sensor inputs and to tune how their signals are conditioned. For example, the interface might need to implement a variety of filters to cope with different input types. But this is a situation where full programmability may not be the most cost-effective option. Some vendors have developed with specific applications in mind that have more limited configurability.

FPAA examples

An example is Analog Devices' SWIO product line, which uses on-chip, sometimes with the help of external passives, to let a variety of sensor interfaces and instruments that signal using 4-20mA current loops to feed data to its digital processor. According to Analog, the driving force for their SWIO product line is a transition to Ethernet that the industrial automation industry is going through. On one side, companies that need to support legacy analogue instrumentation are trying to reduce the number of platforms they need to support. Having a single board design that is able to cater for the wide variety of sensor interfaces could save millions of dollars in development in situations where vendors have to support tens of different I/O combinations. A second driver is the Ethernet transition itself, by allowing factory owners to keep 4-20mA instruments in place but have them talk to systems using the digital network. Equipment makers can, in principle, provide a single configurable module to support the changeover.

Maxim Integrated's PIXI family was developed originally to provide a way to bias the power amplifiers in wireless transceiver designs to help overcome the inventory problem that sector has with the sheer range of radio bands in use around the world. In addition to dedicated temperature sensors, parts such as the MAX11300 employ onchip ADCs and DACs multiplexed across a number of channels to measure and generate different voltages.

Dialog Semiconductor's GreenPak offers a combination of digital sequencing and real-time analogue programmability with the provision of on-chip op-amps and rheostats combined with digital lookup tables. The parts are designed to be able to enable and disable analogue macrocells so that the analogue interfaces are only active and drawing power when needed. The PSoC developed by Cypress Semiconductor, which is now part of Infineon Technologies, couples its programmable-analogue macro cells to a microcontroller to support more complex control scenarios.

Changing systems design

One argument for programmable analogue finally beginning to break out is not so much a desire to cut inventory for designs like industrial sensors but a change in systems design, led by the currently fashionable technology of machine learning. Most machine learning algorithms use some kind of linear algebra for numerical analysis, whether it's for gradient descent in neuron networks or some other kind of iterative optimisation.

Professor Jennifer Hasler of the Georgia Institute of Technology argues that though some numerical analysis methods, such as matrix factorisation are far easier on digital hardware, there are functions that analogue circuitry can potentially do far more efficiently. They include optimisation and differentiation. Early analogue computers were called upon to do those jobs to handle control loops in the absence of fast digital computers.

Though digital logic still has an advantage in terms of speed and density for most jobs, analogue computing has the potential to leap ahead in terms of energy efficiency, at least for the right jobs. In one experiment by Hasler's group, an FPAA was able to recognise command words in speech, taking just 1µJ per inference, or about a thousand times less than similar digital implementations. The FPAA implemented a bank of bandpass filters that were used for feature extraction, feeding into a simple machine-learning algorithm based on an analogue matrix multiplier and a winner-take-all classifier that converted spectral inputs into a few selected symbols.

Now in its third generation, the Georgia Tech RASP work started as blocks of sub-circuits that could be combined in different ways using capacitance in a different way to the switched-capacitor implementations. Here the capacitance being exploited is in the floating gates of transistors developed for non-volatile memory. These are not new to FPGAs. Microsemi's devices have exploited this technology for some though most other FPGAs use SRAM cells to program the connections between configurable elements as well as the entries in their core lookup tables but can only reliably hold digital values. Floating-gate switches on the other hand are capable of holding analogue values, though with limited resolution and accuracy.

The most recent form of the Georgia Tech work implements 600,000 programmable parameters using a relatively old 350nm CMOS process. The floating gates can perform double duties in that many of them are used in the routing fabric but can be programmed to be partially on and so adjust the signal levels that reach destination blocks. Similar to the approach used in analogue AI devices such as those made by Mythic, the analogue nature of the interconnect matrix lets it perform tasks such as matrix multiplication simply by mixing input signals at crosspoints.

Start-up Aspinity has taken a more explicit approach to applying analogue circuitry to machine learning. Its RAMP device uses analogue circuitry operating in the subthreshold regime to save power with the aim of implementing neuromorphic functions. Whereas the Mythic architecture focuses squarely on analogue matrix arithmetic, the Aspinity AnalogML cores include interface functions to connect to sensors and other input devices and blocks that can be configured to perform feature extraction before passing the results to an inferencing core.

Source:https://www.newelectronics.co.uk/electronics-technology/analogue-programmability/236023/