Vidya Vikas Education Trust's
Universal College of Engineering
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## *Department Vision:*

To be recognized for practicing the best teaching-learning methods to create highly competent, resourceful and self-motivated young electronics engineers for benefit of society.

## *Department Mission:*

- To nurture engineers who can serve needs of society using new and innovative techniques in electronics.
- To improve and apply knowledge of electronics subjects through participation in different technical events.
- To enhance carrier opportunities of electronic students through industry interactions and in plant training.
- To install the passion and spirit among students to pursue higher education in electronics and entrepreneurship.

# *New opportunities for medical devices*

This past year saw the COVID-19 pandemic put the future of healthcare, and healthcare technology specifically, under a microscope.

Leading the way on that future is connected health, which looks to offload the healthcare system through self-monitoring Internet of Things (IoT) connectivity, which has been made possible by new innovations like Bluetooth Low Energy (BLE) devices.

Whether it's a smart thermometer automatically feeding data back to a hospital's cloud, or connected blood pressure meters that measure blood pressure readings over a longer period of time, the benefits of BLE make these applications viable thanks to a combination of low power requirements, disposable batteries, affordability, small solution size, built-in security and extensive IoT connectivity.

The IoT has already begun creating new opportunities for medical devices to help doctors improve patient care, and with new innovations like BLE, these devices are improving dramatically. Take wearables, such as a wristband style blood pressure meter, as an example. Wearables and connected health go hand-in-hand. Today, if you need your blood pressure measured, typically you have it done at the doctor's office. But for many patients, a trip to the doctor's office, no matter what the reason, is not exactly a relaxed, care-free time. The stress of being in a doctor's office alone might elevate a patient's blood pressure reading higher than usual, resulting in inaccurate numbers.

With the help of BLE via a sensor node controller, patients can use a connected blood pressure meter at home, helping to ensure a more typically at-rest blood pressure reading, which is then transmitted straight to the cloud for your doctor's office to access. That's higher-quality information for both the doctor and the patient, leading to more accurate diagnoses and prescriptions.

Diabetics are another group of patients that can benefit from innovations in BLE. There is a clear trend away from traditional blood glucose monitors toward glucose meter patches, which don't require patients to prick their fingers. Instead, injection devices such as insulin pens use BLE to send dosage and time stamp data, next to monitored glucose levels from patches, automatically to a Smartphone app for self-monitoring and a doctor's office or hospital, ensuring that healthcare providers are kept apprised of any changes as they occur in real-time. Not only is this a pain-free, longer-lasting alternative, it's also a new way of gathering and storing data about patients' glucose levels in real time, made conveniently accessible right on their phones for easy reference later on.

Smart inhalers are another example of how BLE and IoT connectivity are improving medical devices. Traditional inhalers require asthma patients to wait about 30-60 seconds in between puffs for the medication to go into effect. But studies have found that 84% of patients weren't waiting 30 seconds (the bare minimum recommended time) in between inhalations. The majority of patients

(54%) didn't even wait 15 seconds between puffs, meaning they likely are not receiving their proper dosage of medicine.

As a result, inhalers aren't as effective as they need to be, and the patient has no idea because they don't have a doctor on-hand to provide immediate feedback. With the help of BLE, smart inhalers can address this problem, measuring the device's usage in real-time and providing feedback about the effectiveness of a patient's inhalations, the dosage they're receiving and how frequently they're receiving it.

If there is an underlying theme connecting devices such as wearables, smart glucose monitors and inhalers, it is that they are all able to be improved via the implementation of BLE. BLE devices with IoT connectivity have created the opportunity for remote self-monitoring, allowing patients and their caregivers to monitor their health and manage conditions at home.

Historically, connected medical device engineers have been challenged by a number of factors, such as cost and power availability.

For example, the bill of materials, for both the SoC and external components needed to design a smart blood pressure meter or smart inhaler, has been a major roadblock for engineers trying to deliver meaningful connectivity for these applications.

Meanwhile, power consumption and shelf life have also been major design hurdles.

Medical devices often have long shelf lives, lasting anywhere between 18 months and four years. If the SoC is not consuming power efficiently it simply won't be able to keep up with user needs.

**Tackling these challenges**

To overcome these challenges, back in November 2019, Dialog introduced the DA14531. As the world's smallest and most power-efficient Bluetooth 5.1 SoC, the DA14531 SoC and DA14531 module were designed specifically to simplify Bluetooth product development and enable wider adoption in industries such as healthcare.

The chip, also known as SmartBond TINY lowers the threshold in terms of cost of adding BLE functionality to a level where it's not any longer prohibitive, even not for disposables. an application to as little as $0.50 in high volumes. The SoC's high level of integration only requires six external passives, a single clock source and a power supply to make a complete Bluetooth low energy system. Combined with its ultra-small form factor of just 2.0 x 1.7 mm, the SmartBond TINY can easily fit into any medical device engineer's design.

SmartBond TINY is based on a powerful 32-bit ARM Cortex M0+ with integrated memories and a complete set of analogue and digital peripherals, delivering a record score of 18300 on the latest IoTMark-BLE, the EEMBC benchmark for IoT connectivity. Its architecture and resources allow it to be used as a standalone wireless microcontroller or as an RF data pipe extension for designs with existing microcontrollers.

TINY's low power consumption also ensures a long operating and shelf life, even while powered by the smallest of batteries. The DA14531's integrated DC-DC converter enables a wide operating voltage (1.1 to 3.3V) and derives power directly from environmentally-friendly, disposable silver oxide, zinc air or printable batteries required for high-volume applications, such as smart glucose monitors.

**The future of BLE connectivity**

As the list of devices requiring wireless connectivity continues to grow, so does pressure and cost of delivering a complete IoT system with medical applications. SmartBond TINY looks to address the growing breadth and costs of IoT devices by enabling a complete system cost reduction through a smaller footprint and size, while maintaining performance quality at a level unmatched by competitors.

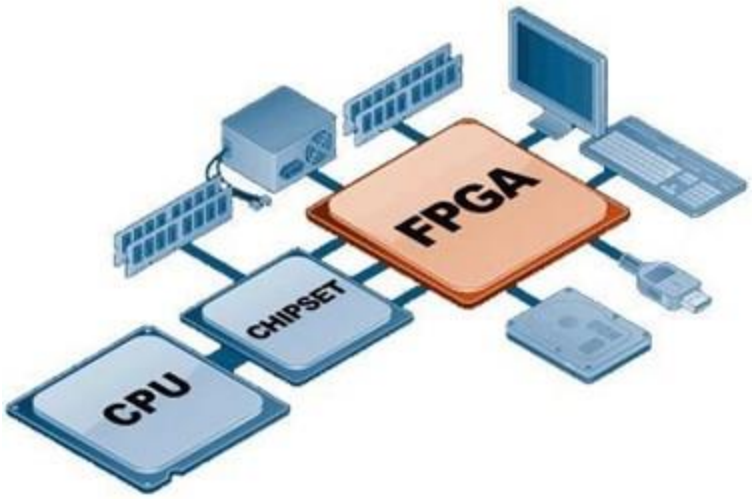
The DA14531 makes it possible to extend wireless connectivity to applications where it would have previously been prohibitive in terms of size, power or cost, especially those within the growing connected medical field. In instances where wearable products will be considered to support medical monitoring functions, the DA1469x family is a perfect choice – it is fully equipped with an on-board sensor node controller and all functionality required for wearable-on-chip designs.

From blood pressure wearables to Smartphone-connected glucose monitoring and connected inhalers, the number of connected medical devices that are possible is limitless - and so is the opportunity for innovating patients' quality of life with BLE.

With the ability to turn any device into a connected application, the TINY SoC and module are opening new markets and driving the adoption of BLE beyond what was previously thought possible in today's landscape.

*Source: https://www.newelectronics.co.uk/electronics-technology/new-opportunities-for-medical-devices/235239/*

# *Addressing safety critical FPGA designs*

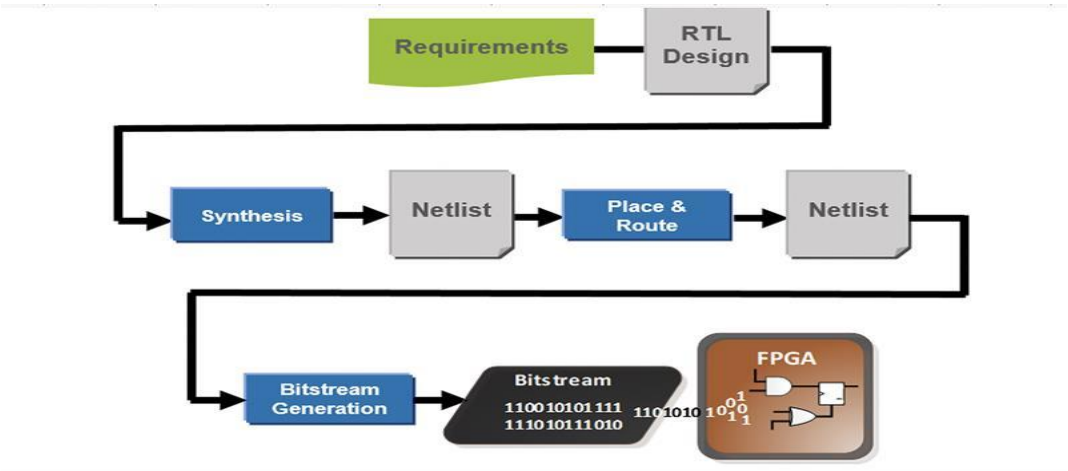



Field-programmable gate arrays (FPGAs) are the dominant hardware platform in many safety-critical, low-volume applications, including aerospace and nuclear power plants (NPPs).

Modern FPGA devices feature integrated microprocessor cores, digital signal processing (DSP) units, memory blocks and other specialised intellectual properties (IPs) and these advanced devices allow for the implementation of large, high-performance system-on-chip (SoC) designs with integrated safety mechanisms, making a strong case for adoption in additional safety-critical applications traditionally dominated by application-specific integrated circuits (ASICs).

From a high-level perspective, the FPGA and ASIC development flows are similar. Register-transfer level (RTL) coding and integration of third-party intellectual properties (IPs) are crucial steps in the front-end part of the flow. Extensive functional verification of the RTL design model reduces the risk of mismatches between requirements and RTL behaviour. At this stage, specification, coding, and module integration mistakes are the main source of systematic faults that, if undetected, could lead to dangerous failures of the FPGA device in the field.

The RTL model then goes through several implementation steps (see below). Synthesis and place-and-route tools map the design onto the target FPGA device. The bitstream generation step produces the file used to program the FPGA. Functional verification of implementation steps reduces the risk of mismatches between the derived netlists and the RTL design model. This is crucial to close the loop and ensure that the functionality implemented in the FPGA device matches the hardware requirements.




*Above: The FPGA development flow*

Functional bugs can be introduced during implementation steps, either because of RTL issues that cannot be detected during synthesis, or because of malfunctions in implementation tools, particularly synthesis and place-and-route, corrupting the original RTL functionality. While engineers may expect that implementation tools have been extensively tested prior to release, each design and coding style are unique and may trigger unknown corner cases.

Regardless of the implementation tool used, there are coding issues that may go undetected during RTL verification and creep into the synthesis

netlist. In some corner case scenarios, RTL simulation behaviour may not match the behaviour of the corresponding netlist in the presence of unknown, or X, values. Consequently, while the synthesis tool operates correctly, its generated netlist may still not match the intended RTL behaviour.

Requirement-based testing does not explicitly target these type of corner cases, which can therefore be missed. RTL linting tools may warn about these scenarios. However, they provide neither a definite answer nor a simulation trace that shows how the bad scenarios may occur.

**Desired functionality**

FPGA implementation tools must fit the desired functionality into a prefabricated structure while meeting performance and power consumption goals. Implementation tools perform significant changes to the original logic structure of the design to improve device utilization and overall quality of results (QoR). Advanced optimisations pose a higher risk of corrupting the RTL functionality.

Certain FPGA synthesis tools support the automatic insertion of hardware safety mechanisms. Safety mechanisms shall not change the design functionality when no fault is present. In the event of a random hardware fault occurring during field operation, they need to raise an alarm and potentially correct the effects of the fault on the fly.

Synthesis tools may transform the encoding of finite state machines (FSMs), for example to include Hamming-based error detection and correction. Triple modular redundancy (TMR) is another type of safety mechanism where a critical logic function is triplicated and voting logic added to determine which of the three outputs should be considered as correct. Logic duplication and inference of memories with error correcting codes (ECC) may also be supported. Users certainly benefit significantly from these design enhancements that can be performed automatically by the synthesis tool. However, the inserted logic could contain bugs and must be rigorously verified.

An effective verification flow must detect bugs as soon as possible once they are introduced. Detecting an RTL issue or synthesis bug during lab testing or Gate Level Simulation (GLS) of the place-and-route netlist is inefficient. Moreover, the effect of bugs introduced by implementation tools is unpredictable. Simulation tests are not intended to verify the correctness of the implementation tools, and even running all available tests at gate-level only provides limited confidence. This approach is indeed far from exhaustive. Finally, debugging GLS and lab test failures is hard and time consuming.

Formal methods are widely recognised as a powerful and exhaustive verification technology. Formal design inspection and exploration is valued for detecting both basic and corner-case RTL issues early and without the need for a simulation testbench.

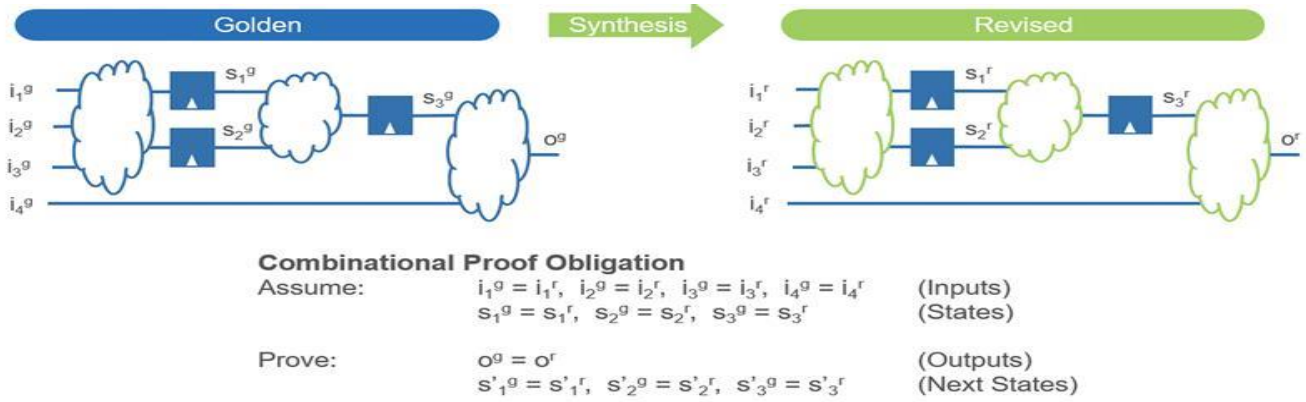
Automated, formal inspection of RTL code detects issues before synthesis starts. Unlike linting, formal tools provide a definite answer on whether an array may be indexed out of bounds. In this

case, the tool provides an easy-to-debug simulation-like trace, or counterexample, that demonstrates how the design misbehaves.

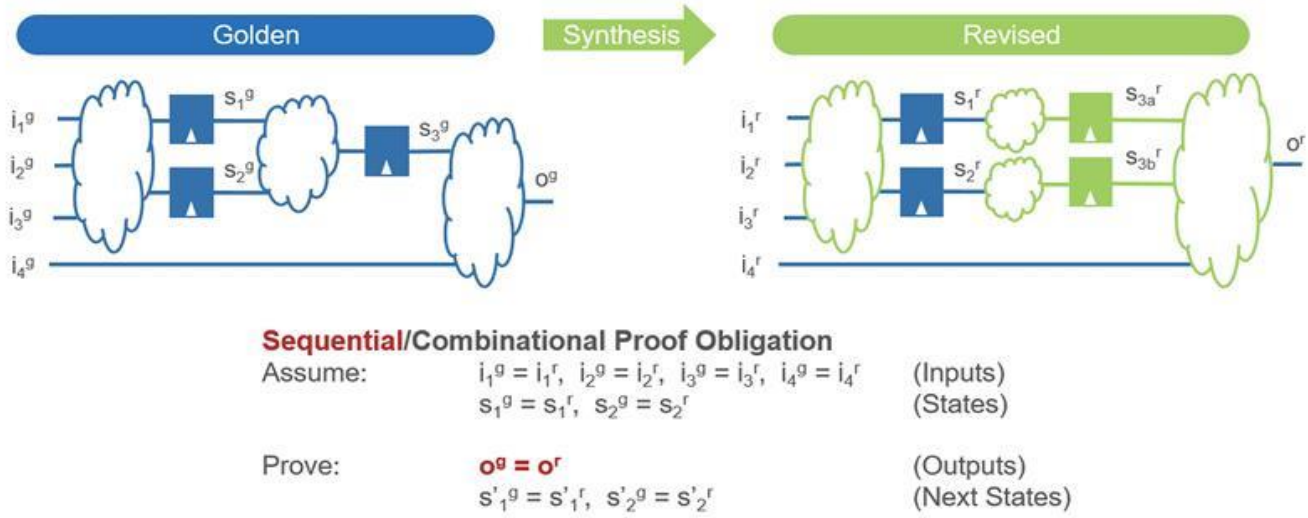
**EC tools**

Formal EC tools can mathematically prove (or disprove) that two designs are functionally equivalent. This is the most rigorous way to ensure that synthesis and other implementation steps have not introduced bugs. The input design to the implementation tool is typically named golden design. The generated netlist is named revised design.

Combinational EC largely relies on one-to-one mapping of states between golden (e.g., the RTL) and revised (e.g., post-synthesis netlist) designs. Through state mapping, the complex problem of proving that two large designs are functionally equivalent can be split into a multitude of much simpler problems: comparing the functionality of two combinational logic cones.

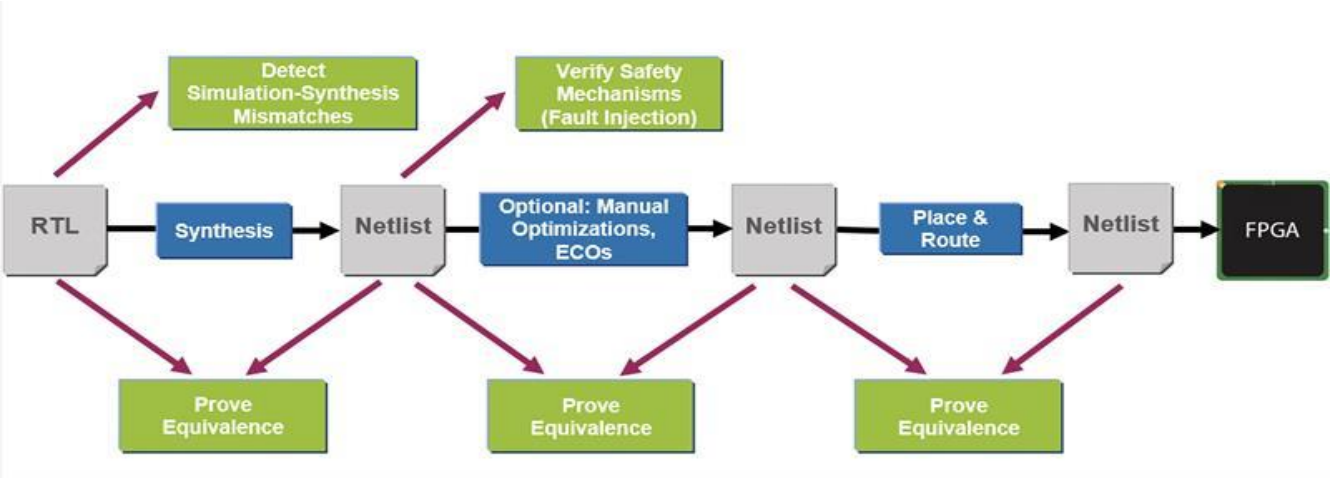



The design transformations performed by FPGA implementation tools significantly break one-to-one state mapping. Formal sequential EC algorithms can prove equivalence of sequential logic cones, thus not requiring state mapping. However, while these algorithms have improved dramatically in recent years, they do not scale. Partial state mapping is necessary to leverage combinational EC wherever possible and apply sequential algorithms only on limited design portions. In this context, identifying corresponding states is a crucial, challenging task. Manual mapping is tedious and time-consuming. Mistakes waste engineering resources.




*Above: These figures show proof obligation in sequential and obligational equivalence checking*

Formal verification signoff enables engineers to use advanced FPGA optimizations and the latest synthesis technology with confidence. Formal RTL design inspection is more powerful than linting and finds issues early, prior to synthesis. Formal EC proves that the golden design functionality is not corrupted by the implementation step. Finally, formal fault injection and verification supported by specialized safety tools, can automate the verification of safety mechanisms in the scenarios when faults occur. With this flow, weeks of GLS and lab testing can be replaced with hours of formal tool runtime.




*Above: Functional sign-off of FPGA implementation with formal verification*

FPGAs have long been the hardware platform of choice in many low-volume safety-critical applications. Nowadays, these devices can implement complex functions while fulfilling tough performance and power goals, competing with ASICs also on high-volume safety-critical applications, including automotive.

The availability of advanced EDA tools and methodology is crucial to support this trend. ASIC development has used formal EC for nearly 20 years. Automated formal checks prior to synthesis are also widely adopted by ASIC teams. The same technology is now available in FPGA development, enabling a robust, efficient implementation process. OneSpin's formal signoff flow of FPGA implementation has been designed to be orders of magnitude more rigorous and efficient than GLS and lab tests. The technology is mature and proven on hundreds of industrial designs for communications, NPPs, and other safety-critical applications.

*Source: https://www.newelectronics.co.uk/electronics-technology/addressing-safety-critical-fpga-designs/235317/*

# *Communication in Fieldbus and Industrial Ethernet standards LAPP industrial cables*

As the production lines develop and become increasingly complex, the number of devices (sensors and actuators) that need to be managed also grows. Industrial processes are carried out by PLCs and extensive networks of digital or analogue connections. Most often, these are systems based on electric (copper) or fibre-optic cables. Depending on the age of the infrastructure, these will be FIELDBUS (older) or ETHERNET (newer) systems

*FIELDBUS_cables_and_connectors*

Numerous plants employ both types of communication networks. Their maintenance and expansion requires the use of special cables, strictly dedicated to a specific data transmission protocol. In addition, this cabling has to be selected depending on the conditions on the operated production line. **Contact with oils, high temperature or the continuous bending of the cable** during operation implies the use of products that are specially adapted for this purpose.

What Fieldbus communication standards are available?

There are several dozen different FIELDBUS transmission protocols available on the market. Among them, it is worth distinguishing three most common types.

- **PROFIBUS® DP** – one of the most popular systems, associated with SIEMENS, but it is based on an openly published model. Numerous manufacturers offer compatible devices and accessories. **Well-scalable**, it offers a wide range of transmission speeds and, consequently,

single cable lengths (up to 1200m). Applied in most industries. A special version dedicated to process automation (**refineries, chemical industry**) called **PROFIBUS® PA8** is also available.

- **CANopen** –a standard that was originally developed for automotive applications. Still commonly used in the automotive industry. With its help, car service technicians conduct computerized diagnostics of the vehicle – however, **it has a much wider application in the automotive industry**. After being extended with a communication profile, it was introduced into industrial automation as CANopen. It is mainly used in Europe, whereas overseas, thanks to Rockwell Automation, it became the **DeviceNet** standard.

- The **CC-Link** standard is most popular among users from Japan and other Asian countries. It has a simple structure and offers easy integration of components from different manufacturers, so it is also frequently chosen by European users.

There are also a few other systems applied in production lines: **Actuator Sensor Interface**, better known as **AS-I, INTERBUS, FOUNDATION Fieldbus** or a very popular **Modbus** system.

Which industrial Ethernet technologies are the best?

In the era of the so-called **Industry 4.0** we are witnessing a tremendous increase in the number of devices connected to the industrial network. **The capacity of FIELDBUS systems** is becoming insufficient. That is why it was necessary to introduce new solutions. Traditional office Ethernet was not suitable for industrial applications, mainly due to signal transmission time lags. They can reach up to 500ms, while production lines with **drive control** require **time lags of a few milliseconds**. In other words, real-time operation is necessary. At the beginning of the 21st century, mechanisms were created to allow for short response times of systems based on the Ethernet infrastructure. An idea of the **Industrial Ethernet** emerged.

The cabling of industrial networks must be resistant not only to harsh environmental conditions, but also **protect the transmitted data from electromagnetic interference**. That is why Industrial Ethernet, in contrast to the office network, mainly involves the use of **screened cables or optical fibres**.

Also in this case, we can list several coexisting standards.

- **PROFINET®** is a leading openly published industrial Ethernet standard in Europe. It enables real-time data exchange between control devices and on-site devices. PROFINET® is the successor to PROFIBUS®.

- **Modbus TCP** is an interesting example of adaptation of the popular FIELDBUS standard. The Modbus data frame has been "packed" into an Ethernet frame to create an open system that has now become one of the standards in process automation.

- **EtherNET/IP** is an industrial bus system used in control and automation systems, mainly in the USA. One of the key advantages of this open standard is the ease of integration of existing on-site devices with a serial RS interface.

- **CC-Link IE** is the leading Ethernet-based standard in Asia, the successor to the CC-Link Fieldbus system. It is used to manage much larger (compared to its predecessor) data volumes.

- **POWERLINK** is an open, real-time extension of the basic Ethernet technology protocol. It is currently the leading Ethernet system. It works in real time and is used in automation technology.

LAPP cables for Fieldbus and Industrial Ethernet communication

*Ethernet_cables*
*Industrial Ethernet cables.*

Selecting the right cable for your application can be quite a challenge. Therefore, it is worth using a ready-made algorithm and answering some basic questions. The key ones will concern the communication standard. Below, we present subsequent steps that will allow our customers to choose the right product. Just click on the answer to go to the catalogue and get familiar with the relevant TME offer.

1. **What will be the type of connection?**

- Cables **fixed in cable ducts**:
  - UNITRONIC BUS PB
  - ETHERLINE PN Cat. 5
- Cable that **may sometimes be moved**, e.g. when relocating a control panel: UNITRONIC BUS CAN
- Movable connections, e.g.**continuous bending in a chain guide**: ETHERLINE FD

1. Will the **cable be applied outdoors, exposed to UV radiation**?

- Yes, **laid on a cable bridge**: UNITRONIC BUS PA
- Yes, but **it will be movable (also in winter)**: ETHERLINE TORSION

1. What **chemicals will come into contact with the cable**?

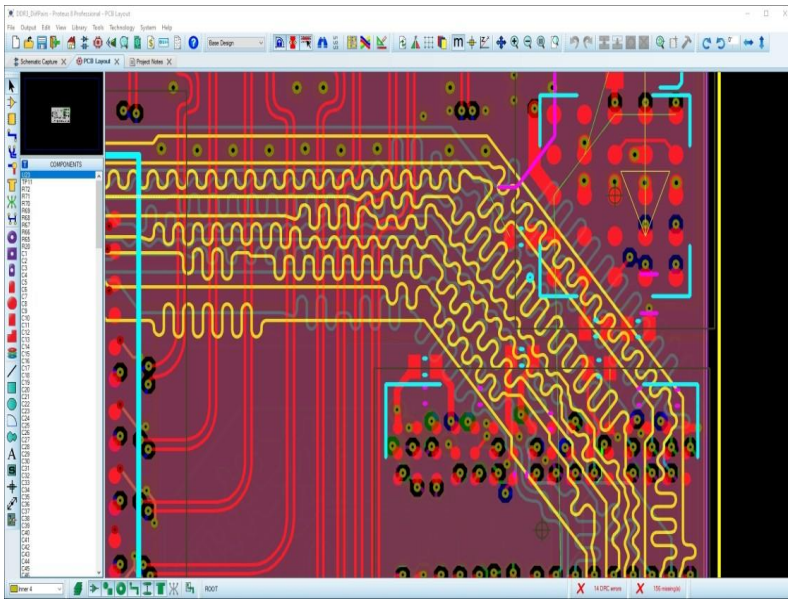
- The cable will be **exposed to oil**: ETHERLINE P
- The cable will be **regularly washed and disinfected, e.g. in a food plant**: ETHERLINE ROBUST
- The cable must be **resistant to contact with boiling water or temperatures up 100°C**: ETHERLINE 105 plus

*Source:* *https://www.newelectronics.co.uk/electronics-technology/communication-in-fieldbus-and-industrial-ethernet-standards-lapp-industrial-cables/235833/*

## *Labcenter Introduces Proteus v8.12 with Enhanced Support for Differential Pair nets and Multi-Board Project Support*

Labcenter Electronics Ltd., the Electronic Design Automation (EDA) company, today announces Proteus v8.12, the latest release of its flagship Proteus Design Suite software. This release sees the completion of support for differential pair routing with pass-through components.

Proteus now enables fast and accurate development of high-speed differential pair signals with automatic skew correction, target length matching and dedicated reporting features. Version 8.12 also sees the start of formal support for multi-board design, where a single schematic encompasses the design logic for multiple PCBs.



In this release, Proteus includes support for multiple rigid boards per project, each of which can have different layer stackups and design rules. Documentation outputs, such as the Bill of Materials, and production outputs, such as Gerber X2, are all board-aware. The design explorer module enables global overview and easy navigation.

"Proteus v8.12 is another important release in our PCB Design technology roadmap," said Iain Cliffe, Executive Director at Labcenter Electronics. "It completes the first phase of work on high speed design support and also introduces dedicated features to support multi-board project design."

*Source:* *https://www.techmezine.com/top-10-news/labcenter-introduces-proteus-v8-12-enhanced-support-differential-pair-nets-multi-board-project-support/*