Vidya Vikas Education Trust's
Universal College of Engineering
Approved by AICTE, DTE, Maharashtra State Goverment and Affiliated to Mumbai University
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Department Vision:

To be recognized for practicing the best teaching-learning methods to create highly competent, resourceful and self-motivated young electronics engineers for benefit of society.

Department Mission:

- To nurture engineers who can serve needs of society using new and innovative techniques in electronics.
- To improve and apply knowledge of electronics subjects through participation in different technical events.
- To enhance carrier opportunities of electronic students through industry interactions and in plant training.
- To install the passion and spirit among students to pursue higher education in electronics and entrepreneurship.

The Race toward Room-temperature Superconductors Heats Up

Superconducting materials are hailed as the “holy grail” of condensed matter physics since their applications are so extensive. From levitating trains and quantum computing to faster and more efficient classical electronics, superconductivity is heavily researched for the swathe of use cases that could transform by vanquishing electrical resistance and magnetic field.

Yet, conventional methods to obtain superconductivity are far from economical, requiring massive amounts of energy and cryogenic cooling. Hence, the next step to achieve affordable and useful superconductivity is to reach superconductivity at higher temperatures (any temperature above 90K (−183°C) in superconductors is considered "high") with the eventual goal being room temperature.

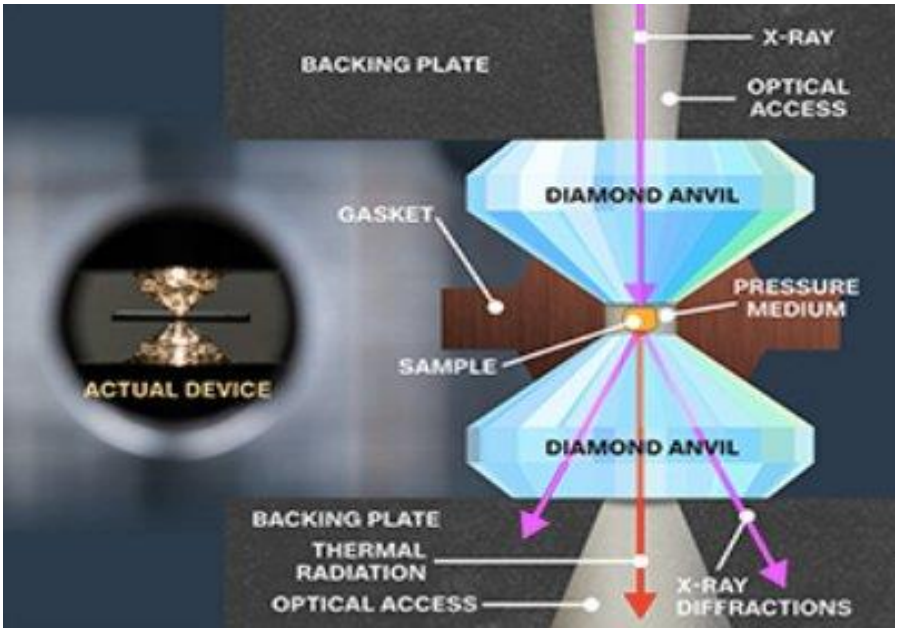
Some of the top electrical engineering research institutions have published new findings on this goal in the past few months, with achievements hailing from the University of Rochester, MIT, and Yale.

The "World’s First Room-temperature Superconductor"

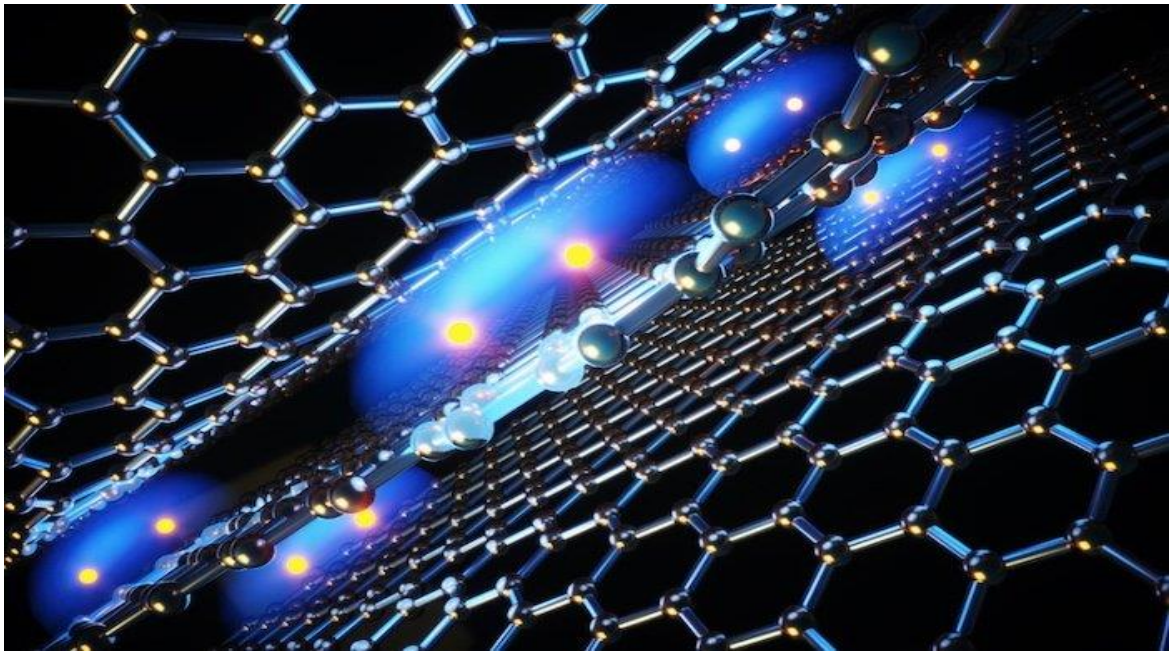
In October, researchers at the University of Rochester achieved what they say is the world’s first room-temperature superconductor.

Instead of achieving superconductivity by means of cooling, the researchers were able to achieve this temperature feat by applying extremely high pressures to a hydrogen-rich material that mimics the lightweight and strong-bond characteristics of pure hydrogen—a strong candidate for high-temperature superconductors.

This material made of yttrium and hydrogen ("yttrium superhydride"), which can be metalized at significantly lower pressures, exhibited a pressure of 26 million pounds per square inch and a record high temperature of 12°F.



MIT Devises a Three-Layer Graphene "Sandwich": While the University of Rochester's findings are a significant step forward to reach superconductivity, the high pressures required still limit the feasibility of this technique in the real world. Earlier this month, MIT researchers published a paper that describes a method for obtaining superconductivity at high temperatures without requiring immense pressure.



In 2018, researchers were able to show that when two thin films of graphene are placed on top of one another at a specific angle, the structure actually becomes a superconductor. Since then, the search for more materials sharing this property has proven fruitless—until now.

Now, the same MIT researchers have been able to observe superconductivity in a three-layer graphene "sandwich," the middle layer of which is twisted at a new angle with respect to the outer layers.

Compared to the original two-layer superconductive material, which has a critical temperature of 1K, the new three-layer material has shown a critical temperature of 3K. As for the exact reason, the scientists are still unsure. "For the moment we have a correlation, not a causation," the researchers noted in a university press release.

Reimaging Coulomb's Law for High-temperature Superconductors:

More superconductor news emerged from Yale University this month, where researchers published a study that challenges fundamental understandings of electromagnetics in superconductors.

Their study, which was focused on high-temperature superconductors, found that in this state the behavior of electrons does not follow Coulomb's law. Normally, two electrons typically repel one another, working to move to the place of lowest energy between one another (which is theoretically infinity).

$$\mathbf{F} = k\frac{q_1 q_2}{r^2}\hat{\mathbf{r}}$$

where…

$k_e = 8.99 \times 10^9\ \mathrm{N\,m^2/C^2}$

is the electrostatic constant

$$\mathbf{F} = \frac{1}{4\pi\varepsilon_0}\frac{q_1 q_2}{r^2}\hat{\mathbf{r}}$$

where…

$\varepsilon_0 = 8.85 \times 10^{-12}\ \mathrm{C^2/N\,m^2}$

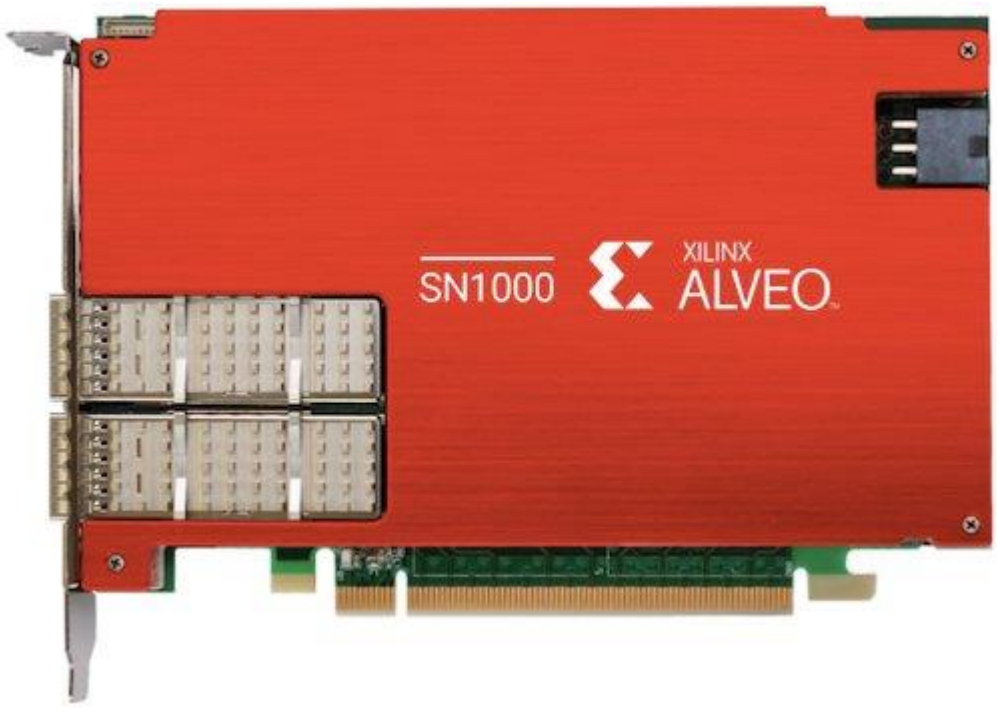
is the vacuum permittivity

Surprisingly, the Yale researchers found that in high-temperature superconductors, electrons behave independently from other atomic particles, creating a ring-like structure with each other.

This is fundamentally opposed to previous understandings of Coulomb's law: instead of moving infinitely away from one another, the electrons move close together, forming a ring-like structure. The researchers theorize that this unprecedented effect may be caused by the "underlying functional form of the Coulomb interaction between valence electrons."

Xilinx Doubles Down on Data Center "Composability" With Accessible SmartNIC

A composable architecture accelerates the modern data center. Xilinx's new SN1000 is said to enhance cloud processor flexibility and operate as an edge device. In preparation for the Xilinx Adapt Virtual Technology Series (March 24–25, 2021), the Xilinx Data Center Group has unveiled a new hardware platform, the Alveo SN1000 SmartNIC, as well as "Smart World" AI video analytics, low-latency electronic trading, and the Xilinx FPGA app store. According to Xilinx, the SN1000 is the industry's first fully-composable SmartNIC solution, capable of adapting to changing data center requirements as quickly as it takes to deploy new software revisions.



The new Xilinx Alveo 100 Gb/s "composable" SN1000 PCIe card. Image used courtesy of Xilinx

Will Composable Architecture Drive the Future of Data Centers?

In an All About Circuits briefing with Xilinx representatives, VP of Marketing Pejman Roshan revealed the pain points the new Alveo SN1000 is solving. "I could have an entire data center that can run a single app on Monday and overnight switch to a completely different application on Tuesday," Roshan explains. "That different application might have different compute requirements, different storage requirements, and different networking requirements."

A solution to these conflicting requirements, Xilinx asserts, is composable architectures.

IBM defines composable architectures as logical software building blocks that deliver functions such as compute, storage, and networking—but with the added ability to provision new infrastructure on demand.

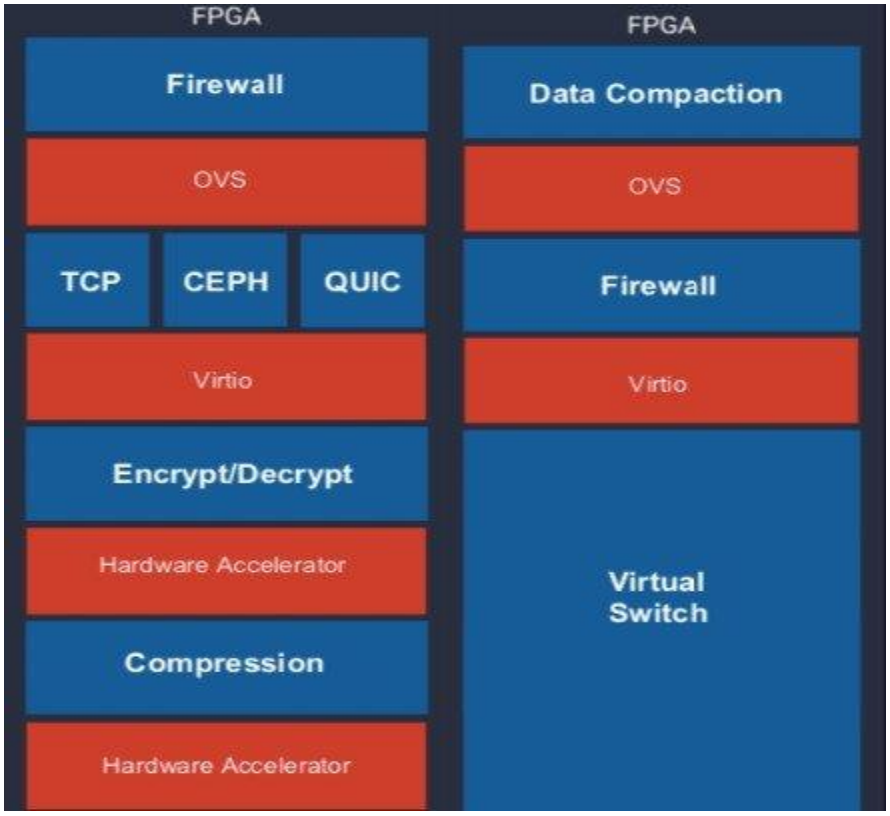
Composability is a key feature that ties together all the Xilinx solutions released today.

New SmartNIC Places Composability as Centerpiece

ASIC implementations, as well as CPU/SoC architectures, simply fall short of the flexibility requirements in the dynamic modern data center. The reason for this limitation is simple. There are many market hyperscalers and cloud service providers who all have different requirements in compute, network, and storage.

Kartik Srinivasan, Networking and Storage Business Lead for the Xilinx Data Center Group, says that composability is the biggest distinction between this SmartNIC and others.

The SN1000 is a PCIe packaged in a full-height, half-length standardized form factor, which consumes up to 75 W, offering two-channel 100 Gb off-load capability.



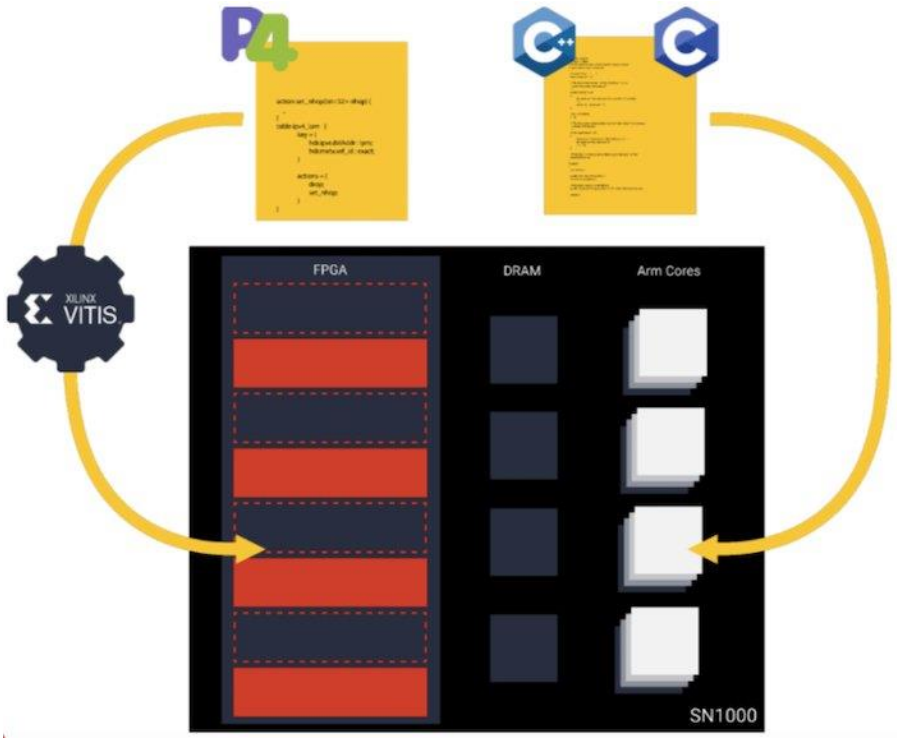
Two examples of composability (red) and flexibility in base FPGA architecture (blue), which may allow engineers to build custom off-loads or extend existing IP. Image (modified) courtesy of Xilinx

The card itself is based upon the Xilinx 16nm UltraScale+ FPGA fabric and a 16-core Arm processor. Xilinx explains that the FPGA fabric is the source of the composability for the SN1000, offering flexible offloading requirements related to networking, security, and storage.

Software-defined Hardware? FPGA Development for all Engineers

While FPGAs are (typically) notoriously difficult to program, Xilinx says it has built accessibility into the hardware-level of the SN1000. Further, the SmartNIC acknowledges that workhorse languages for FPGA development, Verilog and VHDL RTL, are still alive and kicking.

Xilinx is combining its Vitis development platform with higher-level languages like the P4 codebase to streamline data-plane development. This may ease engineers who are more accustomed to higher-level software development into FPGA development.



By abstracting away the complexity of bare-metal programming in favor of high-level languages, Xilinx says it is introducing FPGAs to a new generation of engineers. Image used courtesy of Xilinx

Software teams already familiar with development on the Arm platforms with C and C++ can more easily come up to speed with P4 and Vitis to program the data-plane features of the FPGA.

Perks of Alveo Hardware for Edge Compute

In the past year, data centers have undergone heightened demand for bandwidth and data processing as many employees have begun working from home to combat the pandemic. One way to alleviate this burden is through edge device hardware acceleration.

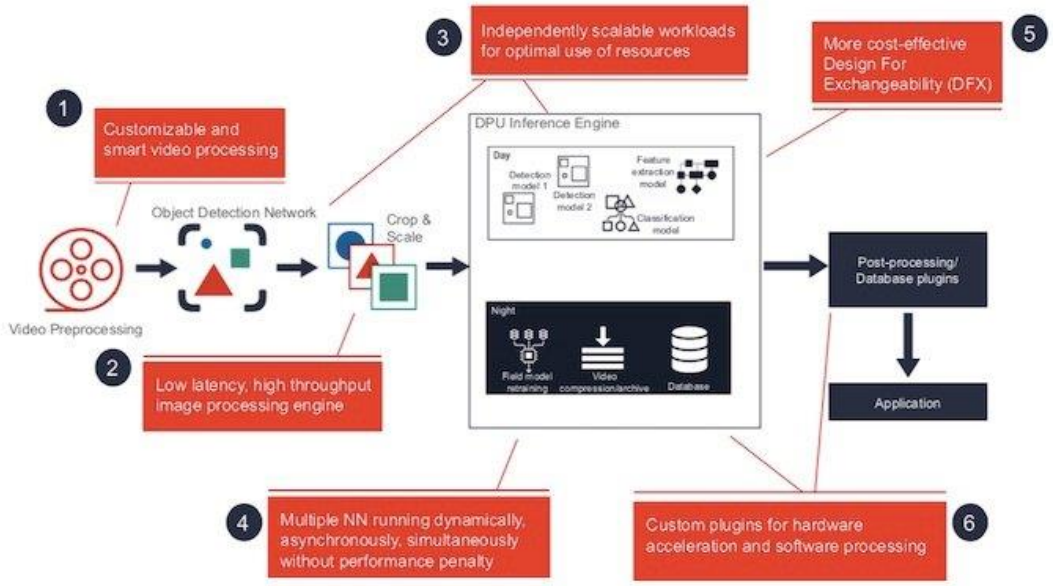
Xilinx says its Alveo product family of hardware accelerator devices can benefit multiple industries:

- Global incident and emergency management systems
- Worker safety
- Retail loss prevention (due to errors and misappropriation)
- Hospital response and monitoring

The Push for Composable Data Centers and Accessible FPGAs

FPGAs, which Xilinx has described as "born to run" in data centers, are uniquely suited to provide massively-parallel data processing. This capability reduces the total cost of ownership of edge-compute devices and improves performance with a low-latency response.

As an example of a success story, Xilinx claims that the Tencent Cloud Service Provider was able to reduce its bandwidth costs by 90% between edge and cloud by combining technologies from Xilinx and partner Aupera.



High-performance edge-device video analytic compute capability, deployable "out-of-the-box" with the Alveo product family. Image used courtesy of Xilinx

The new Xilinx launch of the Alveo SN1000 indicates two major trends involving data center hardware. First, the concept of composability may be the key to driving data center agility. The announcement also reveals how FPGA development is going mainstream with higher-level abstraction of the hardware, which eases development.

Source: https://www.allaboutcircuits.com/news/xilinx-doubles-down-data-center-composability-accessible-smartnic/