University of Mumbai
Examination June 2021
Examinations Commencing from 1st June 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev2016

Examination: BE Semester VI

Course Code: ELX603 and Course Name: VLSI Design

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	In full adders the sum circuit is implemented using _____
Option A:	AND & OR gates
Option B:	XOR
Option C:	NAND gate
Option D:	XNOR
2.	Which is the storage element in DRAM?
Option A:	Inductor
Option B:	capacitor
Option C:	Resistor
Option D:	Mosfet
3.	The biggest disadvantage of Ripple carry adder is
Option A:	simple design
Option B:	easy to implement
Option C:	propagation delay
Option D:	extra hardware requirement
4.	The biggest advantage of carry lookahead adder is
Option A:	simple design
Option B:	easy to implement
Option C:	Very small propagation delay
Option D:	extra hardware requirement
5.	Which one is not a feature of SRAM?
Option A:	Low power consumption
Option B:	Refresh operations required
Option C:	volatile memory
Option D:	low cell density
6.	Which one is not a feature of DRAM?
Option A:	Low power consumption
Option B:	Refresh operations required
Option C:	volatile memory

Option D:	high cell density
7.	Which one is not defined in manchester carry adder?
Option A:	carry skip
Option B:	carry propagate
Option C:	carry generate
Option D:	carry kill
8.	NAND flash memory is based on arranging ___ mosfets in series.
Option A:	6
Option B:	4
Option C:	8 or 16
Option D:	32
9.	Working of Flash memory is based on the absence/presence of electrons in
Option A:	control gate
Option B:	Source
Option C:	floating gate
Option D:	Drain
10.	Carry look ahead adder cannot be implemented by
Option A:	static CMOS logic
Option B:	Mirror circuit
Option C:	Multiple output domino logic(MODL)
Option D:	pass transistor logic
11.	The VIL is found from transfer characteristic of inverter by
Option A:	The point where the straight line at VOH ends
Option B:	The slope of the transition at a point at which the slope is equal to -1
Option C:	The midpoint of the transition line
Option D:	All of the mentioned
12.	The Lower Noise Margin is given by:
Option A:	VOL – VIL
Option B:	VIL – VOL
Option C:	VIL ~ VOL(Difference between VIL and VOL, depends on which one is greater)
Option D:	All of the Mentioned
13.	The noise immunity with noise margin.
Option A:	Decreases
Option B:	Increases
Option C:	Constant
Option D:	Cant say
14.	If n-transistor conducts and has large voltage between source and drain, then it is said to be in region.
Option A:	linear region
Option B:	saturation region
Option C:	non saturation

Option D:	cut-off
15.	CMOS inverter has _____ output impedance.
Option A:	Low
Option B:	High
Option C:	Very high
Option D:	None of these
16.	What is the input resistance of CMOS inverter?
Option A:	Low
Option B:	High
Option C:	Very low
Option D:	None of these
17.	The junction parasitic capacitance are produced due to
Option A:	Source diffusion regions
Option B:	Gate diffusion regions
Option C:	Drain diffusion region
Option D:	Body diffusion region
18.	Register cell consists of
Option A:	Inverter
Option B:	pass transistor
Option C:	inverter & pass transistor
Option D:	None of these
19.	In clocked CMOS logic, output in evaluated in
Option A:	on period
Option B:	Off period
Option C:	Both the period
Option D:	Half the on period
20.	CMOS domino logic occupies compared to static CMOS design
Option A:	smaller area
Option B:	larger area
Option C:	Equal area
Option D:	Depends on implemented logic

Q2	
A	**Solve any Two** **5 marks each**
i.	Explain MOSFET capacitance.
ii.	Short note on level 1 and level 2 mosfet models.
iii.	Explain .
B	**Solve any One** **10 marks each**
i.	Derive critical voltages level for CMOS inverter.
ii.	Explain working of 6T SRAM.

Q3	
A	**Solve any Two** **5 marks each**
i.	Explain working of flash memory.
ii.	Explain Manchester Adder.
iii.	Explain ESD.
B	**Solve any One** **10 marks each**
i.	Explain DRAM read write operations.
ii.	Explain clock generation, stabilization and distribution.