University of Mumbai
Examination 2020

Examinations Commencing from 7th January 2021 to 20th January 2021

Program: **Information Technology Engineering**

Curriculum Scheme: **Rev2016**

Examination: **TE** Semester **V**

Course Code: **ITC501** and Course Name: **Microcontroller and Embedded Programming**

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called?
Option A:	fragmentation
Option B:	paging
Option C:	mapping
Option D:	none of the mentioned
2.	How many bits of offset are used in the conditional branching?
Option A:	24
Option B:	32
Option C:	16
Option D:	8
3.	XRL, ORL, ANL commands have _____
Option A:	accumulator as the destination address and any register, memory or any immediate data as the source address
Option B:	accumulator as the destination address and any immediate data as the source address
Option C:	any register as the destination address and accumulator, memory or any immediate data as the source address
Option D:	any register as the destination address and any immediate data as the source address
4.	Which of the following bits are set for Serial port interrupt generation?
Option A:	IE
Option B:	RI, IE
Option C:	IP, TI
Option D:	RI, TI
5.	A valid division instruction always makes:
Option A:	CY=0, AC=1
Option B:	CY=1, AC=1
Option C:	CY=0, AC=0
Option D:	Does not affect AC and CY flags
6.	Which of the following registers are not bit addressable?
Option A:	SCON

Option B:	PCON
Option C:	A
Option D:	PSW
7.	When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?
Option A:	PSW
Option B:	SP
Option C:	DPTR
Option D:	PC
8.	The SP is of ___ wide register. And this may be defined anywhere in the _____.
Option A:	8 byte, on-chip 128 byte RAM
Option B:	8 bit, on chip 256 byte RAM
Option C:	16 bit, on-chip 128 byte ROM
Option D:	8 bit, on chip 128 byte RAM
9.	What is the time taken by one machine cycle if crystal frequency is 20MHz?
Option A:	1.085 micro seconds
Option B:	0.60 micro seconds
Option C:	0.75 micro seconds
Option D:	1 micro seconds
10.	What is the meaning of the instruction MOV A, 05H?
Option A:	data 05H is stored in the accumulator
Option B:	fifth bit of accumulator is set to one
Option C:	address 05H is stored in the accumulator
Option D:	none of the mentioned
11.	The Instruction, LDM R10!, {R0,R1,R6,R7} _____
Option A:	Loads the contents of R10 into R1, R0, R6 and R7
Option B:	Creates a copy of the contents of R10 in the other registers except for the above mentioned ones
Option C:	Loads the contents of the registers R1, R0, R6 and R7 to R10
Option D:	Writes the contents of R10 into the above mentioned registers and clears R10
12.	The instruction, MLA R0,R1,R2,R3 performs:
Option A:	R0 ← [R1]+[R2]+[R3]
Option B:	R3 ← [R0]+[R1]+[R2]
Option C:	R0 ← [R1]*[R2]+[R3]
Option D:	R3 ← [R0]*[R1]+[R2]
13.	Do the two instructions mean the same? 1) BACK: DEC R0 JZ BACK 2) BACK: DJNZ RO, BACK
Option A:	YES
Option B:	NO
Option C:	can't be determined
Option D:	yes and the second one is preferred

14.	CJNE instruction makes _____
Option A:	the pointer to jump if the values of the destination and the source address are equal
Option B:	sets CY=1, if the contents of the destination register are greater then that of the source register
Option C:	sets CY=0, if the contents of the destination register are smaller then that of the source register
Option D:	none of the mentioned
15.	Which part of the software is transparent to the interrupt mechanism?
Option A:	background
Option B:	foreground
Option C:	both background and foreground
Option D:	lateral ground
16.	CPU fetches the instruction from memory according to the value of _____
Option A:	program counter
Option B:	status register
Option C:	instruction register
Option D:	program status word
17.	Which one of the following is the address generated by CPU?
Option A:	physical address
Option B:	absolute address
Option C:	logical address
Option D:	none of the mentioned
18.	The ability to shift or rotate in the same instruction along with other operation is performed with the help of
Option A:	Switching circuit
Option B:	Barrel switcher circuit
Option C:	Integrated Switching circuit
Option D:	Multiplexer circuit
19.	Which instruction is used to get the 1's complement of the operand?
Option A:	COMP
Option B:	BIC
Option C:	~CMP
Option D:	MVN
20.	Which pin of port 3 is has an alternative function as write control signal for external data memory?
Option A:	P3.8
Option B:	P3.3
Option C:	P3.6
Option D:	P3.1

Q2 (20 Marks)	**Solve any Four out of Six.**
A	Differentiate between Microprocessor and Microcontrollers.
B	Give salient features of ARM7 processor.
C	Explain in brief various characteristics of RTOS.
D	What are the design metrics of an embedded system.
E	List some important features of Raspberry_Pi board.
F	Explain modes of timers in 8051.

Q3.(20 Marks)	**Solve any Two Questions out of Three.**
A	Write a program to transfer “INDIA” serially at 9600 baud rate using 8051.Assume frequency 11.0592MHz.
B	List and explain how exceptions and interrupts handled in ARM7.
C	Draw interfacing of keyboard matrix with 8051 in detail with diagram. Write a program to generate Hexadecimal values.