University of Mumbai

Examination 2020

Examinations Commencing from 7th January 2021 to 20th January 2021

Program: Information Technology Engineering

Curriculum Scheme: Rev2016

Examination: TE Semester V

Course Code: **ITC501** and Course Name: **Microcontroller and Embedded Programming** Time: 2 hour Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called?
Option A:	fragmentation
Option B:	paging
Option C:	mapping
Option D:	none of the mentioned
2.	How many bits of offset are used in the conditional branching?
Option A:	24
Option B:	32
Option C:	16
Option D:	8
3.	XRL, ORL, ANL commands have
Option A:	accumulator as the destination address and any register, memory or any
• P · · · · · ·	immediate data as the source address
Option B:	accumulator as the destination address and any immediate data as the source address
Option C:	any register as the destination address and accumulator, memory or any immediate data as the source address
Option D:	any register as the destination address and any immediate data as the source address
4.	Which of the following bits are set for Serial port interrupt generation?
Option A:	IE
Option B:	RI, IE
Option C:	IP, TI
Option D:	RI, TI
5	A valid division instruction always makes:
J. Option A:	A valid division instruction always makes. CV=0 $AC=1$
Option R:	$C_1 = 0, AC = 1$
Option C:	$\begin{array}{c} C 1^{-1}, A C^{-1} \\ C V = 0 A C = 0 \end{array}$
Option D:	Does not affect AC and CV flags
Option D:	
6.	Which of the following registers are not bit addressable?
Option A:	SCON

Option B:	PCON
Option C:	A
Option D:	PSW
7.	When the microcontroller executes some arithmetic operations, then the flag bits
	of which register are affected?
Option A:	PSW
Option B:	SP
Option C:	DPTR
Option D:	PC
8.	The SP is of wide register. And this may be defined anywhere in the
Option A:	8 byte, on-chip 128 byte RAM
Option B:	8 bit, on chip 256 byte RAM
Option C:	16 bit, on-chip 128 byte ROM
Option D:	8 bit, on chip 128 byte RAM
9.	What is the time taken by one machine cycle if crystal frequency is 20MHz?
Option A:	1.085 micro seconds
Option B:	0.60 micro seconds
Option C:	0.75 micro seconds
Option D:	1 micro seconds
10.	What is the meaning of the instruction MOV A, 05H?
Option A:	data 05H is stored in the accumulator
Option B:	fifth bit of accumulator is set to one
Option C:	address 05H is stored in the accumulator
Option D:	none of the mentioned
	The Instruction, LDM R10!, $\{R0,R1,R6,R7\}$
Option A:	Loads the contents of R10 into R1, R0, R6 and R7
Option B:	Creates a copy of the contents of R10 in the other registers except for the above
	mentioned ones
Option C:	Loads the contents of the registers R1, R0, R6 and R/ to R10
Option D:	Writes the contents of R10 into the above mentioned registers and clears R10
12	The instruction MIA DO D1 D2 D2 nonformed
12.	$P_{0} = [P_{1}] + [P_{2}] + [P_{2}]$
Option R:	$R_{0} = [R_{1}] + [R_{2}] + [R_{3}]$
Option C:	$K_{3} \leftarrow [K_{0}]^{+}[K_{1}]^{+}[K_{2}]$
Option D:	$R_{1} \leftarrow [R_{1}] + [R_{2}] + [R_{3}]$
Option D.	
13	Do the two instructions mean the same?
15.	1) BACK · DEC R0
	JZ BACK
	2) BACK: DJNZ RO. BACK
Option A [.]	YES
Option B:	NO
Option C:	can't be determined
Option D:	ves and the second one is preferred
·	· 1

14. CJNE instruction makes Option A: the pointer to jump if the values of the destination and the source address are equal Option B: sets CY=0, if the contents of the destination register are greater then that of the source register Option D: none of the mentioned 15. Which part of the software is transparent to the interrupt mechanism? Option D: none of the mentioned 0ption B: foreground Option D: hackground and foreground Option D: lateral ground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: instruction register Option D: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option D: none of the creati Option A: Switching circuit Option D: Multiplexer circuit Option B: B		
Option A: the pointer to jump if the values of the destination and the source address are equal Option B: sets CY=0, if the contents of the destination register are greater then that of the source register Option D: sets CY=0, if the contents of the destination register are smaller then that of the source register Option D: none of the mentioned Image: the source register the source register Option D: none of the mentioned Image: the source register the software is transparent to the interrupt mechanism? Option A: background Option D: lateral ground Option D: lateral ground Option C: istatus register Option A: program counter Option D: program status word Image: the solution of the following is the address generated by CPU? Option A: physical address Option C: logical address Option D: none of the mentioned Image: the solut address the solut address Option A: physical address Option C: logical address Option C: logical address Option A: Switching circuit	14.	CJNE instruction makes
Option B: sets CY=1, if the contents of the destination register are greater then that of the source register Option C: sets CY=0, if the contents of the destination register are smaller then that of the source register Option D: none of the mentioned 15. Which part of the software is transparent to the interrupt mechanism? Option B: foreground Option D: background and foreground Option D: lateral ground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option B: status register Option D: instruction register Option D: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switching circuit Option B: Barrel switching circuit Option B: Barrel switching circuit Option B: BIC Option B: <td>Option A:</td> <td>the pointer to jump if the values of the destination and the source address are equal</td>	Option A:	the pointer to jump if the values of the destination and the source address are equal
Option C: sets CY=0, if the contents of the destination register are smaller then that of the source register Option D: none of the mentioned 15. Which part of the software is transparent to the interrupt mechanism? Option B: foreground Option D: lateral ground Option D: lateral ground Option D: lateral ground Option D: lateral ground I6. CPU fetches the instruction from memory according to the value of Option B: status register Option D: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option B: absolute address Option D: none of the mentioned 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barcl switching circuit <	Option B:	sets CY=1, if the contents of the destination register are greater then that of the source register
Option D: none of the mentioned 15. Which part of the software is transparent to the interrupt mechanism? Option A: background Option A: program counter Option A: program counter Option A: program counter Option D: instruction register Option D: program counter Option A: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit 0ption A: Switching circuit Option B: BIC Option B: BIC Option B: BIC	Option C:	sets CY=0, if the contents of the destination register are smaller then that of the source register
15. Which part of the software is transparent to the interrupt mechanism? Option A: background Option B: foreground Option D: lateral ground Option D: lateral ground Option D: lateral ground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: instruction register Option D: instruction register Option C: logical address Option C: logical address Option D: none of the following is the address generated by CPU? Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option B: Barcel switching circuit Option A: COMP Option B: BIC Option B: BIC Option B: BIC Option B: BIC Option B: BIC <td>Ontion D:</td> <td>none of the mentioned</td>	Ontion D:	none of the mentioned
15. Which part of the software is transparent to the interrupt mechanism? Option A: background Option D: lateral ground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: instruction register Option D: program status register Option D: program status word 17. Which one of the following is the address generated by CPU? Option B: absolute address Option D: none of the mentioned 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option A: Switching circuit Option B: Barcel switcher circuit Option D: Multiplexer circuit Option D: Multiplexer circuit	Option D.	
Option A: background Option B: foreground Option C: both background and foreground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option B: status register Option D: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option D: Nultiplexer circuit Option D: Multiplexer circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit Option D: Which instruction is used to get the 1's complement of the operand? Option A: COMP Option D: MVN 19. Which in of port 3 is has an alternative function as write control signal for external data memory? Option D: MVN	15.	Which part of the software is transparent to the interrupt mechanism?
Option B: foreground Option C: both background and foreground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: status register Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: absolute address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option D: Switching circuit Option D: Multiplexer circuit 0ption B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option C:	Option A:	background
Option C: both background and foreground Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: status register Option D: instruction register Option D: program status word 17. Which one of the following is the address generated by CPU? Option B: absolute address Option D: physical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switching circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option D: BIC Option D: MVN <td>Option B:</td> <td>foreground</td>	Option B:	foreground
Option D: lateral ground 16. CPU fetches the instruction from memory according to the value of Option A: program counter Option D: status register Option D: program counter Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 17. Which one of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option D: Multiplexer circuit 0ption D: Multiplexer circuit 0ption D: MUN 20. Which instruction is used to get the 1's complement of the operand? Option D: BIC Option D: MUN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option B: P3.8 Opt	Option C [.]	both background and foreground
Image: Second	Option D:	lateral ground
16. CPU fetches the instruction from memory according to the value of Option A: program counter Option B: status register Option C: instruction register Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: absolute address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option D: P3.4 Option D: P3.6 Option D: P3.6 Option D: P3.1	option D.	
Option A: program counter Option B: status register Option C: instruction register Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: none of the mentioned 0 instruction rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option A: Switching circuit Option D: Multiplexer circuit Option B: Barrel switcher circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option D: P3.4 Option D: P3.6 Option D: P3.1	16.	CPU fetches the instruction from memory according to the value of
Option B: status register Option C: instruction register Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switcher circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option D: Multiplexer circuit 0ption B: BIC Option D: - 19. Which instruction is used to get the 1's complement of the operand? Option B: BIC Option D: - QPI - 0ption D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option D: P3.4 Option D:	Option A:	program counter
Option C: instruction register Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: absolute address Option C: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switching circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option B: BIC Option A: COMP Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option B: P3.8 Option D: P3.4	Option B:	status register
Option D: program status word 17. Which one of the following is the address generated by CPU? Option A: physical address Option B: absolute address Option D: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switcher circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option B: P3.8 Option D: P3.6 Option D: P3.1	Option C:	instruction register
17. Which one of the following is the address generated by CPU? Option A: physical address Option B: absolute address Option C: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option B: P3.8 Option C: P3.6 Option D: P3.1	Option D:	program status word
 17. Which one of the following is the address generated by CPU? Option A: physical address Option D: absolute address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1 	•	
Option A: physical address Option B: absolute address Option C: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option D: Multiplexer circuit Option D: Multiplexer circuit Option A: COMP Option A: COMP Option B: BIC Option C: ~CMP Option D: Mvich instruction is used to get the 1's complement of the operand? Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	17.	Which one of the following is the address generated by CPU?
Option B: absolute address Option C: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option A:	physical address
Option C: logical address Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option D: MUK 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option B:	absolute address
Option D: none of the mentioned 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option D: Integrated Switching circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option C:	logical address
18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option D: Multiplexer circuit Option A: COMP Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.1	Option D:	none of the mentioned
 18. The ability to shift or rotate in the same instruction along with other operation is performed with the help of Option A: Switching circuit Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit 19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1 		
Option A: Switching circuit Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit 19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option D: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option D: P3.1	18.	The ability to shift or rotate in the same instruction along with other operation is performed with the help of
Option B: Barrel switcher circuit Option C: Integrated Switching circuit Option D: Multiplexer circuit 19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option D: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option D: P3.1	Option A:	Switching circuit
Option C: Integrated Switching circuit Option D: Multiplexer circuit 19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option B:	Barrel switcher circuit
Option D: Multiplexer circuit 19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option B: BIC Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option B: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option C:	Integrated Switching circuit
19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option D:	Multiplexer circuit
19. Which instruction is used to get the 1's complement of the operand? Option A: COMP Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1		
Option A: COMP Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option C: P3.6 Option D: P3.1	19.	Which instruction is used to get the 1's complement of the operand?
Option B: BIC Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option D: P3.3 Option C: P3.6 Option D: P3.1	Option A:	COMP
Option C: ~CMP Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option B:	BIC
Option D: MVN 20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option C:	~CMP
20. Which pin of port 3 is has an alternative function as write control signal for external data memory? Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1	Option D:	MVN
20.Which pin of port 3 is has an alternative function as write control signal for external data memory?Option A:P3.8Option B:P3.3Option C:P3.6Option D:P3.1	I	
external data memory?Option A:P3.8Option B:P3.3Option C:P3.6Option D:P3.1	20.	Which pin of port 3 is has an alternative function as write control signal for
Option A: P3.8 Option B: P3.3 Option C: P3.6 Option D: P3.1		external data memory?
Option B: P3.3 Option C: P3.6 Option D: P3.1	Option A:	P3.8
Option C: P3.6 Option D: P3.1	Option B:	P3.3
Option D: P3.1	Option C:	P3.6
	Option D:	P3.1

Q2 (20 Marks)	Solve any Four out of Six.
А	Differentiate between Microprocessor and Microcontrollers.
В	Give salient features of ARM7 processor.
С	Explain in brief various characteristics of RTOS.
D	What are the design metrics of an embedded system.
E	List some important features of Raspberry_Pi board.
F	Explain modes of timers in 8051.

Q3.(20 Marks)	Solve any Two Questions out of Three.
•	Write a program to transfer "INDIA" serially at 9600 baud rate using
A	8051.Assume frequency 11.0592MHz.
В	List and explain how exceptions and interrupts handled in ARM7.
С	Draw interfacing of keyboard matrix with 8051 in detail with diagram.
C	Write a program to generate Hexadecimal values.