University of Mumbai

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: **Computer Engineering**

Curriculum Scheme: **Rev2016**

Examination: **TE** Semester **V**

Course Code: **CSC501** and Course Name: **Microprocessor**

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	_____ is the most important segment and it contains the actual assembly language instructions to be executed by the microprocessor.
Option A:	Data segment
Option B:	Code segment
Option C:	Stack segment
Option D:	Extra segment
2.	A0 pin of 8086 is used for selecting the data from
Option A:	Even bank
Option B:	Odd bank
Option C:	Both
Option D:	Parity bank
3.	The Instruction Pointer is _____ bits in length
Option A:	8 bits
Option B:	4 bits
Option C:	16 bits
Option D:	32 bits
4.	The index register is used to hold _____.
Option A:	Segment memory
Option B:	Offset memory
Option C:	Offset address
Option D:	Segment address
5.	**Which of the following is not a machine control flag?**
Option A:	Direction flag
Option B:	Interrupt flag
Option C:	Overflow flag
Option D:	Trap flag
6.	**In 8086 the overflow flag is set when_____.**
Option A:	The sum is more than 16 bit
Option B:	Carry and sign flags are set
Option C:	Signed numbers go out of their range after an arithmetic operation

Option D:	During subtraction
7.	CMC instruction is used to
Option A:	Compare carry flag
Option B:	Set carry flag
Option C:	Reset carry flag
Option D:	Complement carry flag
8.	EQU assembler directive is used to
Option A:	Give a name to some value or to a symbol.
Option B:	Assign value to integer
Option C:	Assign value to character
Option D:	Assign a value to floating point no.
9.	80386 supports ___ stages integer pipeline
Option A:	4 stages
Option B:	8 stages
Option C:	5 stages
Option D:	10 stages
10.	Pentium supports following bits of address bus
Option A:	32 bit
Option B:	64 bit
Option C:	16 bit
Option D:	128 bit
11.	The result of the CMP instruction is stored in
Option A:	Source operand
Option B:	Destination operand
Option C:	Flag register
Option D:	Accumulator
12.	Auto EOI mode of 8259 PIC is also called as _____ mode
Option A:	Automatic Rotation
Option B:	Specific Rotation
Option C:	Non Specific EOI
Option D:	Specific EOI
13.	IMR register of 8259 is used to set
Option A:	Mask Mode
Option B:	Buffered Mode
Option C:	Cascade Mode
Option D:	Poll command Mode
14.	8259 resolves the priority of the interrupt which should be raised to processor
Option A:	Priority resolver
Option B:	Interrupt mask register
Option C:	Interrupt service register

Option D:	Interrupt control register
15.	The pin that disables all the DMA channels by clearing the mode registers is
Option A:	Mark
Option B:	Clear
Option C:	Reset
Option D:	Ready
16.	The segments in 80386 real mode are
Option A:	Overlapped
Option B:	non-overlapped
Option C:	either overlapped
Option D:	semi overlapped
17.	Port C of 8255 can function independently as
Option A:	input port
Option B:	output port
Option C:	either input or output ports
Option D:	both input and output ports
18.	In 8257 (DMA), each of the four channels has
Option A:	a pair of two 8-bit registers
Option B:	a pair of two 16-bit registers
Option C:	one 16-bit register
Option D:	one 8-bit register
19.	The common register(s) for all the four channels of 8257 is
Option A:	DMA address register
Option B:	Terminal count register
Option C:	Mode set register and status register
Option D:	Task set register
20.	The unit that is disabled in real address mode is
Option A:	central processing unit
Option B:	memory management unit
Option C:	paging unit
Option D:	bus control unit

Q2 **(20 Marks)**	**Solve any Two** **5 marks each**
A	
i.	Write addressing modes of the following instructions i) MOV AX, [BX+SI] ii) AND CL,[2000]

	iii) IN AL, DX iv) JMP [BX+2] v) ADD AX,[BX+SI+5]
ii.	Write short note on Mixed language programming
iii.	Differentiate real mode, protected mode and virtual mode of 80386 microprocessor
B	**Solve any One** **10 marks each**
i.	Draw and explain demultiplexing of address bus in 8086
ii.	Explain how flushing of pipeline problem is minimized in Pentium architecture.

Q3 (20 Marks)	**Solve any Two** **5 marks each**
A	
i.	Explain VM, RF, IOPL and NT flags of 80386 microprocessor
ii.	Write short note on types of interrupts
iii.	Give the advantages of memory segmentation of 8086 microprocessor
B	**Solve any One** **10 marks each**
i.	Draw and explain the block diagram of 8255 Programmable Peripheral Interface (PPI) with control word formats.
ii.	Explain different addressing modes of 8086 microprocessor.