# University of Mumbai
# Examination 2020

Program: Electronics and Telecommunication Engineering
Curriculum Scheme: Rev2012
Examination: Third Year Semester VI
Course Code: ETC606 and Course Name: VLSI Design

Time: 1 hour                                                                 Max. Marks: 50

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For the students:- All the Questions are compulsory and carry equal marks .

| Q1. | The scaling factor similar to scaling factor of power speed product is: |
| --- | --- |
| Option A: | Power dissipation per unit area |
| Option B: | Switching Energy |
| Option C: | Power dissipation per gate |
| Option D: | Power dissipation of the device |
| | |
| Q2. | Increasing fan-out _____ the propagation delay. |
| Option A: | increases |
| Option B: | decreases |
| Option C: | does not affect |
| Option D: | exponentially decreases |
| | |
| Q3. | Which of the following capacitor can store more data in DRAM? |
| Option A: | planar capacitor |
| Option B: | trench capacitor |
| Option C: | stacked-cell |
| Option D: | non-polar capacitor |
| | |
| Q4. | The final addition sum of the numbers, 0110 & 0110 is _____ |
| Option A: | 1101 |
| Option B: | 1111 |
| Option C: | 1001 |
| Option D: | 1010 |
| | |
| Q5. | In consistency/ justification, tracking is done |
| Option A: | forward from gate input to primary input |
| Option B: | backwards from gate input to primary output |
| Option C: | backwards from gate input to primary input |
| Option D: | forward from gate output to primary output |
| | |
| Q6. | To propagate the fault along the selected path to primary output, setting _____ is done. |
| Option A: | AND to 1 |
| Option B: | OR to 1 |
| Option C: | NOR to 1 |
| Option D: | NAND to 0 |
| | |
| Q7. | A _____ gate is used to detect the occurrence of an overflow. |
| Option A: | NAND |

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| Option B: | XOR |
| Option C: | XNOR |
| Option D: | AND |
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| Q8. | What is the size of a trench capacitor in DRAM? |
| Option A: | 1 Mb |
| Option B: | 4-256 Mb |
| Option C: | 8-128 Mb |
| Option D: | 64-128 Mb |
| | |
| Q9. | What is the input resistance of CMOS inverter? |
| Option A: | high |
| Option B: | low |
| Option C: | very low |
| Option D: | Cannot be determined |
| | |
| Q10. | The static component of power dissipation is given by: |
| Option A: | $P = I^2.Rd$ |
| Option B: | $P = Vdd^2/Ron$ |
| Option C: | $P = Eg.fo$ |
| Option D: | $P = Eg.Rd$ |
| | |
| Q11. | The gate delay is proportional to: |
| Option A: | Ron.Cg |
| Option B: | Rs.Cds |
| Option C: | Rd.Cgs |
| Option D: | Ron.Cox |
| | |
| Q12. | In CMOS domino logic _____ is possible. |
| Option A: | inverting structure |
| Option B: | non inverting structure |
| Option C: | inverting and non inverting structure |
| Option D: | very complex design |
| | |
| Q13. | How many MOSFETs are required for SRAM? |
| Option A: | 2 |
| Option B: | 4 |
| Option C: | 6 |
| Option D: | 8 |
| | |
| Q14. | Which method is suitable for larger operands? |
| Option A: | Baugh-Wooley algorithm |
| Option B: | Wallace trees |
| Option C: | Dadda multipliers |
| Option D: | Modified booth encoding |
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| Q15. | Oxide breakdown occurs due to |
| Option A: | electrostatic charge |

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| Option B: | threshold voltage |
| Option C: | voltage shift |
| Option D: | poor input/output pad circuitry |
| | |
| Q16. | Exhaustive testing is suitable when N is |
| Option A: | small |
| Option B: | large |
| Option C: | any value for N |
| Option D: | very large |
| | |
| Q17. | In full adders the sum circuit is implemented using _____ |
| Option A: | AND & OR gates |
| Option B: | NAND gate |
| Option C: | XOR |
| Option D: | XNOR |
| | |
| Q18. | Which is the storage element in DRAM? |
| Option A: | inductor |
| Option B: | capacitor |
| Option C: | resistor |
| Option D: | MOSFET |
| | |
| Q19. | In CMOS inverter, transistor is a switch having _____ |
| Option A: | infinite on resistance |
| Option B: | finite off resistance |
| Option C: | buffer |
| Option D: | infinite off resistance |
| | |
| Q20. | The dynamic component of power dissipation is given by: |
| Option A: | $P = I^2.Rd$ |
| Option B: | $P = Vdd^2/Rd$ |
| Option C: | $P = Eg.fo$ |
| Option D: | $P = Eg.Rd$ |
| | |
| Q21. | The power dissipation per gate is scaled as: |
| Option A: | 1 |
| Option B: | $1/ \beta.\alpha^2$ |
| Option C: | $\alpha^2/\beta$ |
| Option D: | $1/ \beta^2$ |
| | |
| Q22. | CMOS inverter has _____ regions of operation. |
| Option A: | three |
| Option B: | four |
| Option C: | two |
| Option D: | five |
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| Q23. | Which memory storage is widely used in PCs and Embedded Systems? |
| Option A: | SRAM |

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| Option B: | DRAM |
| Option C: | Flash memory |
| Option D: | EEPROM |
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| Q24. | Internally, a computer's binary data are always transmitted on parallel channels which is commonly referred to as the _____ |
| Option A: | Parallel bus |
| Option B: | Serial bus |
| Option C: | Data bus |
| Option D: | Memory bus |
| | |
| Q25. | Which model is used for pc board testing? |
| Option A: | stuck at |
| Option B: | stuck in |
| Option C: | stuck on |
| Option D: | stuck through |