University of Mumbai
Examination 2020

Program: BE Information Technology Engineering

Curriculum Scheme: Revised 2016

Examination: Second Year Semester III

Course Code: ITC302 and Course Name: Logic Design

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks.

Q1.	A crystal diode has ……
Option A:	One pn junction
Option B:	Two pn junctions
Option C:	Three pn junctions
Option D:	Five pn junctions
Q2.	If the arrow of crystal diode symbol is positive w.r.t. bar, then diode is …….. Biased.
Option A:	Forward
Option B:	Reverse
Option C:	North
Option D:	base
Q3.	For a BJT, for common base configuration the input characteristics is represented by a plot between which of the following parameters?
Option A:	VBE and IE
Option B:	VBE and IB
Option C:	VCE and IC
Option D:	VCC and IC
Q4.	Determine the early voltage, if the output resistance is 2.5×2kΩ and input current is 2mA
Option A:	9.8v
Option B:	5.6v
Option C:	7.8v
Option D:	10v
Q5.	In practical application of current mirror, early voltage is assumed to be
Option A:	Infinite
Option B:	Zero
Option C:	Unity
Option D:	One
Q6.	Power of binary system for positional value is

Option A:	2
Option B:	10
Option C:	8
Option D:	16
Q7.	The number system which contain 8 different symbols 0, 1, 2, 3, 4, 5, 6, 7 is
Option A:	hexadecimal system
Option B:	binary system
Option C:	octal system
Option D:	quinary system
Q8.	How to represent -9 with signed 2's complement?
Option A:	10001001
Option B:	11110110
Option C:	11110111
Option D:	11110011
Q9.	The binary number 111 in octal format is _____
Option A:	6
Option B:	7
Option C:	8
Option D:	5
Q10.	Convert (22)8 into its corresponding decimal number.
Option A:	28
Option B:	18
Option C:	81
Option D:	82
Q11.	Octal subtraction of (232)8 from (417)8 will give _____
Option A:	165
Option B:	185
Option C:	815
Option D:	516
Q12.	The 1's complement of 0.101 is _____
Option A:	1.010
Option B:	0.010
Option C:	0.101
Option D:	1.101
Q13.	Which of the following code is also known as reflected code?
Option A:	Excess-3 code
Option B:	Gray code

Option C:	Straight binary code
Option D:	Error code
Q14.	The universal gate is ……
Option A:	NAND gate
Option B:	OR gate
Option C:	AND gate
Option D:	Ex-OR gate
Q15.	The following switching functions are to be implemented using a decoder:f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)The minimum configuration of decoder will be _____
Option A:	2 to 4 line
Option B:	3 to 8 line
Option C:	4 to 16 line
Option D:	5 to 32 line
Q16.	How many AND gates are required to realize Y = CD + EF + G?
Option A:	4
Option B:	5
Option C:	3
Option D:	2
Q17.	The NOR gate output will be high if the two inputs are _____
Option A:	00
Option B:	01
Option C:	10
Option D:	11
Q18.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?
Option A:	OR
Option B:	AND
Option C:	XOR
Option D:	NAND
Q19.	A full adder logic circuit will have _____
Option A:	Two inputs and one output
Option B:	Three inputs and three outputs
Option C:	Two inputs and two outputs
Option D:	Three inputs and two outputs

Q20.	The gates required to build a half adder are _____
Option A:	EX-OR gate and NOR gate
Option B:	EX-OR gate and OR gate
Option C:	EX-OR gate and AND gate
Option D:	EX-NOR gate and AND gate
Q21.	Which of the following are building blocks of encoders?
Option A:	NOT gate
Option B:	OR gate
Option C:	AND gate
Option D:	NAND gate
Q22.	Which of the following can be represented for decoder?
Option A:	Sequential circuit
Option B:	Combinational circuit
Option C:	Logical circuit
Option D:	Local circuit
Q23.	What is a multiplexer?
Option A:	It is a type of decoder which decodes several inputs and gives one output
Option B:	A multiplexer is a device which converts many signals into one
Option C:	It takes one input and results into many output
Option D:	It is a type of encoder which decodes several inputs and gives one output
Q24.	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
Option A:	AND or OR gates
Option B:	XOR or XNOR gates
Option C:	NOR or NAND gates
Option D:	AND or NOR gates
Q25.	A package in VHDL consists of _____
Option A:	Commonly used architectures
Option B:	Commonly used tools
Option C:	Commonly used data types and subroutines
Option D:	Commonly used syntax and variables