University of Mumbai
Examination 2020

Program: Electronics Engineering
Curriculum Scheme: Rev2016
Examination: Second Year Semester V
Course Code: EXTC501 and Course Name: Microprocessor and Peripheral Interfacing
Time: 1 hour Max. Marks: 50
Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	8255 consists of _____ 8-bit bidirectional I/O ports
Option A:	2
Option B:	3
Option C:	4
Option D:	5
Q2.	Specify the addressing mode for the instruction: MOV AX,[BX+ 1004H]
Option A:	Immediate Addressing
Option B:	Register Addressing
Option C:	Direct Addressing
Option D:	Register Relative Addressing
Q3.	Which pin is used to indicate use of odd/higher memory bank?
Option A:	ALE
Option B:	BHE
Option C:	DIR
Option D:	VCC
Q4.	Which pin is used to enable latch to hold on the content of address lines?
Option A:	ALE
Option B:	BHE
Option C:	DIR
Option D:	VCC
Q5.	8086 is a _____ bit microprocessor.
Option A:	8
Option B:	16
Option C:	32
Option D:	64
Q6.	What is not present inside the microprocessor?
Option A:	ALU
Option B:	Control Unit
Option C:	Registers
Option D:	I/O devices
Q7.	Banking of memory leads to

Option A:	increase in data access speed
Option B:	decrease in data access speed
Option C:	increase in humidity
Option D:	decrease in temperature
Q8.	Physical address is calculated by
Option A:	physical address = (starting address * 10) + offset address
Option B:	physical address = (starting address * 20) + offset address
Option C:	physical address = (starting address * 10H) + offset address
Option D:	physical address = (offset address * 10 H) + starting address
Q9.	The instruction pointer is default pointer of
Option A:	code segment register
Option B:	data segment register
Option C:	stack segment register
Option D:	extra segment register
Q10.	Destination index is a default pointer of
Option A:	code segment register
Option B:	data segment register
Option C:	stack segment register
Option D:	extra segment register
Q11.	Maximum size of a memory segment is ____ kB
Option A:	64
Option B:	32
Option C:	48
Option D:	16
Q12.	Total number of interrupts in 8086 is
Option A:	32
Option B:	64
Option C:	128
Option D:	256
Q13.	All I/O data transfers using IN and OUT instructions use _____ register
Option A:	A
Option B:	B
Option C:	C
Option D:	D
Q14.	If carry is generated out of lower nibble then _____ flag is set.
Option A:	Carry
Option B:	Parity
Option C:	Auxillary Carry

Option D:	Interrupt
Q15.	To configure 8086 in minimum mode, MN/MX' pin should be connected with _____
Option A:	VCC
Option B:	GND
Option C:	Keep open
Option D:	INTR pin
Q16.	_____ is used to exchange a byte/word between source and destination given in instruction.
Option A:	XLAT
Option B:	MOV
Option C:	PUSH
Option D:	XCHG
Q17.	Identify an invalid logical instruction for 8086.
Option A:	AND
Option B:	OR
Option C:	XNOR
Option D:	XOR
Q18.	After the execution of SHL & SHR instructions, the empty bits are filled with____
Option A:	0
Option B:	1
Option C:	last bit is copied
Option D:	randomly filled
Q19.	NOP stands for
Option A:	No operation performed
Option B:	Number of operations performed
Option C:	number of operations not performed
Option D:	none of these
Q20.	INT 0 is dedicated to _____ interrupt.
Option A:	NMI
Option B:	Overflow
Option C:	divide by 0 error
Option D:	single stepping
Q21.	INT 2 is dedicated to _____ interrupt.
Option A:	NMI
Option B:	Overflow
Option C:	divide by 0 error
Option D:	single stepping

Q22.	which of the following is a hardware interrupt?
Option A:	divide by 0
Option B:	Overflow
Option C:	NMI
Option D:	int 21H
Q23.	8284 clock generator provides ____% duty cycle.
Option A:	25
Option B:	33
Option C:	50
Option D:	75
Q24.	Number of address lines available for I/O devices is
Option A:	8
Option B:	16
Option C:	20
Option D:	32
Q25.	8257 has ___ channels.
Option A:	3
Option B:	4
Option C:	5
Option D:	6