University of Mumbai
Examination 2020

Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	DT/R pin of 8086 is connected to __ pin of 8286
Option A:	OE pin
Option B:	T pin
Option C:	CS pin
Option D:	R pin
Q2.	By using TRAP flag 8086 can
Option A:	Enable the FLAG register
Option B:	Can execute one instruction at a time
Option C:	Can execute group of instruction at a time
Option D:	Can add breakpoint
Q3.	A0 pin of 8086 is used for selecting the data from
Option A:	Even bank
Option B:	Odd bank
Option C:	Both
Option D:	Parity bank
Q4.	Maximum mode of 8086 is
Option A:	Uniprocessor system
Option B:	Multiprocessor system
Option C:	Superscalar system
Option D:	Single processor system
Q5.	With 8086 the use of DX register is to
Option A:	Store count value
Option B:	Store Operations result
Option C:	Store I/O addresses
Option D:	Store data value
Q6.	In 8086 the overflow flag is set when_____.

Option A:	The sum is more than 16 bit
Option B:	Carry and sign flags are set
Option C:	Signed numbers go out of their range after an arithmetic operation
Option D:	During subtraction
Q7.	The instruction, CMP to compare source and destination operands it performs
Option A:	Addition
Option B:	Subtraction
Option C:	Multiplication
Option D:	Division
Q8.	Which of the following instruction is not valid?
Option A:	MOV AX, BX
Option B:	MOV DS, 5000H
Option C:	MOV AX, 5000H
Option D:	PUSH AX
Q9.	The instructions that involve various string manipulation operations are
Option A:	branch instructions
Option B:	flag manipulation instructions
Option C:	shift and rotate instructions
Option D:	string instructions
Q10.	CBW instruction converts
Option A:	Byte to word
Option B:	Word to byte
Option C:	Signed no to unsigned no
Option D:	Unsigned no to signed no
Q11.	Which of the following is conditional branch instruction?
Option A:	CALL
Option B:	Loop
Option C:	JMP
Option D:	JNC
Q12.	When 8259 PIC's SP/EN pin is connected to GND
Option A:	Its Master PIC
Option B:	Its slave PIC
Option C:	Its Core PIC
Option D:	Its basic PIC
Q13.	The fully nested mode of 8259 PIC is also called as
Option A:	Fixed priority mode

Option B:	Rotating Priority mode
Option C:	Automatic rotation
Option D:	Specific rotation
Q14.	While responding to an interrupt 8086 microprocessor doesn't
Option A:	It pushes flags to stack
Option B:	Pushes CS to stack
Option C:	Pushes IP to stack
Option D:	Push the content of general purpose register to stack
Q15.	The Synchronization between microprocessor and memory is done by
Option A:	ALE
Option B:	HOLD
Option C:	READY
Option D:	HLDA
Q16.	Following register of 8237 DMAC is used for storing the no. of bytes to be transferred
Option A:	Address register
Option B:	Word count register
Option C:	Command register
Option D:	Status register
Q17.	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
Option A:	data bus control
Option B:	read logic control
Option C:	control word register
Option D:	address buffers
Q18.	The following mode of 8253 PIT can be used in digital clock
Option A:	Square Wave Generator
Option B:	Programmable Rate Generator
Option C:	Software Triggered Strobe
Option D:	Programmable One Shot
Q19.	In square wave generator mode in case of odd count(N) the output stays high for
Option A:	N+2 clock cycles
Option B:	N-2 clock cycles
Option C:	(N+1)/2 clock cycles
Option D:	(N-1)/2 clock cycles

Q20.	The memory of 80386 was divided into following no of banks
Option A:	2 banks
Option B:	4 banks
Option C:	6 banks
Option D:	8 banks
Q21.	Following control register of 80386 holds the page directory physical base address.
Option A:	CR0
Option B:	CR1
Option C:	CR2
Option D:	CR3
Q22.	The flag register of 80386 is also called as
Option A:	Enabled flag register
Option B:	Extended flag register
Option C:	Emulated flag register
Option D:	Extra flag register
Q23.	The type of execution which means that the CPU should guess which of the next instructions can be executed earlier is
Option A:	speculative execution
Option B:	out of turn execution
Option C:	dual independent bus
Option D:	multiple branch prediction
Q24.	The salient feature of Pentium is
Option A:	superscalar architecture
Option B:	superpipelined architecture
Option C:	superscalar and superpipelined architecture
Option D:	Scalable Architecture
Q25.	The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
Option A:	Prefetch stage
Option B:	D1 (first decode) stage
Option C:	D2 (second decode) stage
Option D:	Final stage