Program: BE Electronics and Telecommunication Engineering
Curriculum Scheme: Revised 2012
Examination: Third Year Semester VI
Course Code: ETC606 and Course Name:VLSI Design

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	MOS transistor structure is _____
Option A:	symmetrical
Option B:	non symmetrical
Option C:	semi symmetrical
Option D:	pseudo symmetrical
Q2.	P-well doping concentration and depth will affect the _____
Option A:	threshold voltage
Option B:	Vss
Option C:	Vdd
Option D:	Vgs
Q3.	In Constant voltage model the gate capacitance is scaled by a factor of:
Option A:	1/β 2
Option B:	1/α 2
Option C:	β/α 2
Option D:	α/β 2
Q4.	The scaling factor of power dissipation per unit area in constant voltage

	model is:
Option A:	1
Option B:	1/α2
Option C:	1/ β.α2
Option D:	α2/β2
Q5.	In CMOS inverter, transistor is a switch having _____
Option A:	infinite on resistance
Option B:	finite off resistance
Option C:	buffer
Option D:	infinite off resistance
Q6.	If βn = βp, then Vin is equal to _____
Option A:	Vdd
Option B:	Vss
Option C:	2Vdd
Option D:	0.5Vdd
Q7.	Mobility depends on _____
Option A:	Transverse electric field
Option B:	Vg
Option C:	Vdd
Option D:	Channel length

Q8.	In CMOS NOR gate, p transistors are connected in
Option A:	series
Option B:	parallel
Option C:	cascade
Option D:	random
Q9.	In CMOS logic circuit the n-MOS transistor acts as:
Option A:	Load
Option B:	Pull up network
Option C:	Pull down network
Option D:	Not used in CMOS circuits
Q10.	In CMOS domino logic _____ is possible.
Option A:	inverting structure
Option B:	non inverting structure
Option C:	inverting and non inverting structure
Option D:	very complex design
Q11.	In CMOS domino logic _____ is used.
Option A:	two phase clock
Option B:	three phase clock
Option C:	one phase clock
Option D:	four phase clock

Q12.	In Pseudo-nMOS logic, n transistor operates in
Option A:	cut off region
Option B:	saturation region
Option C:	resistive region
Option D:	non saturation region
Q13.	In clocked CMOS logic, rise time and fall time are
Option A:	faster
Option B:	slower
Option C:	faster first and then slows down
Option D:	slower first and then speeds up
Q14.	The power dissipation in Pseudo-nMOS is reduced to about _____ compared to nMOS device.
Option A:	50%
Option B:	30%
Option C:	60%
Option D:	70%
Q15.	The full form of EPROM is _____
Option A:	Easy Programmable Read Only Memory
Option B:	Erasable Programmable Read Only Memory
Option C:	Eradicate Programmable Read Only Memory

Option D:	Easy Programmable Read Out Memory
Q16.	RAM is a _____ cell
Option A:	dynamic
Option B:	partially dynamic
Option C:	pseudo static
Option D:	static
Q17.	With the increase of number of cells in array, transistor size will
Option A:	increase
Option B:	decrease
Option C:	remain default
Option D:	doesn't change
Q18.	Minimum time allowed between two consecutive memory operations are called
Option A:	memory access time
Option B:	memory cycle time
Option C:	memory dynamic time
Option D:	memory static time
Q19.	Bulk of memory consists of cells in which
Option A:	bits are stored
Option B:	bits are copied

Option C:	bits are added
Option D:	bits are subtracted
Q20.	What are carry generate combinations?
Option A:	If all the input are same then a carry is generated
Option B:	If all of the output are independent of the inputs
Option C:	If all of the input are dependent on the output
Option D:	If all of the output are dependent on the input
Q21.	In the adder, sum is stored in
Option A:	Series
Option B:	Cascade
Option C:	Parallel
Option D:	Registers
Q22.	A barrel shifter is a _____ based Digital circuit.
Option A:	Adder
Option B:	Encoder
Option C:	Multiplexer
Option D:	Counter
Q23.	What is ripple carry adder?
Option A:	The carry output of the lower order stage is connected to the carry input of the next higher order stage

Option B:	The carry input of the lower order stage is connected to the carry output of the next higher order stage
Option C:	The carry output of the higher order stage is connected to the carry input of the next lower order stage
Option D:	The carry input of the higher order stage is connected to the carry output of the lower order stage
Q24.	Reduction in power dissipation can be brought by
Option A:	increasing transistor area
Option B:	decreasing transistor area
Option C:	increasing transistor feature size
Option D:	decreasing transistor feature size
Q25.	ESD in common terminology refers to _____
Option A:	Electrostatic discharge
Option B:	Electric discharge
Option C:	Electronic discharge
Option D:	Elastic discharge