Program: BE Electronics and Telecommunication Engineering
Curriculum Scheme: Revised 2016
Examination: Third Year Semester VI
Course Code: ECCDLO6021 and Course Name: Digital VLSI Design
Time: 1 hour Max. Marks: 50
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Note to the students:- All the Questions are compulsory and carry equal marks .

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| Q1. | MOS transistor structure is _____ |
| Option A: | symmetrical |
| Option B: | non symmetrical |
| Option C: | semi symmetrical |
| Option D: | pseudo symmetrical |
| | |
| Q2. | RTL is a design abstraction of what kind of circuit? |
| Option A: | Asynchronous digital circuit |
| Option B: | Synchronous digital circuit |
| Option C: | Asynchronous sequential circuit |
| Option D: | Analog circuit |
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| Q3. | What happens if the input is high in FSM? |
| Option A: | Change of state |
| Option B: | No transition in state |
| Option C: | Remains in a single state |
| Option D: | Invalid state |
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| Q4. | In FSM diagram what does circle represent? |
| Option A: | Change of state |
| Option B: | State |
| Option C: | Output value |
| Option D: | Initial state |
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| Q5. | The Complex programmable logic devices contain several PLD blocks and |
| Option A: | Field programmable switches |
| Option B: | AND/OR arrays |
| Option C: | Global Interconnection matrix |
| Option D: | Language compiler |
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| Q6. | What does RTL in digital circuit design stand for? |
| Option A: | Register transfer language |
| Option B: | Register transfer logic |
| Option C: | Register transfer level |
| Option D: | Resistor-transistor logic |
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| Q7. | Which type of device FPGA are? |
| Option A: | SLD |
| Option B: | SROM |
| Option C: | EPROM |
| Option D: | PLD |

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| Q8. | In CMOS NOR gate, p transistors are connected in |
| Option A: | series |
| Option B: | parallel |
| Option C: | cascade |
| Option D: | random |
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| Q9. | In CMOS logic circuit the n-MOS transistor acts as: |
| Option A: | Load |
| Option B: | Pull up network |
| Option C: | Pull down network |
| Option D: | Not used in CMOS circuits |
| | |
| Q10. | In CMOS domino logic _____ is possible. |
| Option A: | inverting structure |
| Option B: | non inverting structure |
| Option C: | inverting and non inverting structure |
| Option D: | very complex design |
| | |
| Q11. | In CMOS domino logic _____ is used. |
| Option A: | two phase clock |
| Option B: | three phase clock |
| Option C: | one phase clock |
| Option D: | four phase clock |

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| Q12. | In Pseudo-nMOS logic, n transistor operates in |
| Option A: | cut off region |
| Option B: | saturation region |
| Option C: | resistive region |
| Option D: | non saturation region |
| | |
| Q13. | In clocked CMOS logic, rise time and fall time are |
| Option A: | faster |
| Option B: | slower |
| Option C: | faster first and then slows down |
| Option D: | slower first and then speeds up |
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| Q14. | The power dissipation in Pseudo-nMOS is reduced to about _____ compared to nMOS device. |
| Option A: | 50% |
| Option B: | 30% |
| Option C: | 60% |
| Option D: | 70% |
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| Q15. | The full form of EPROM is _____ |
| Option A: | Easy Programmable Read Only Memory |
| Option B: | Erasable Programmable Read Only Memory |

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| Option C: | Eradicate Programmable Read Only Memory |
| Option D: | Easy Programmable Read Out Memory |
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| Q16. | RAM is a _____ cell |
| Option A: | dynamic |
| Option B: | partially dynamic |
| Option C: | pseudo static |
| Option D: | static |
| | |
| Q17. | With the increase of number of cells in array, transistor size will |
| Option A: | increase |
| Option B: | decrease |
| Option C: | remain default |
| Option D: | doesn't change |
| | |
| Q18. | Minimum time allowed between two consecutive memory operations are called |
| Option A: | memory access time |
| Option B: | memory cycle time |
| Option C: | memory dynamic time |
| Option D: | memory static time |
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| Q19. | Bulk of memory consists of cells in which |
| Option A: | bits are stored |

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| Option B: | bits are copied |
| Option C: | bits are added |
| Option D: | bits are subtracted |
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| Q20. | What are carry generate combinations? |
| Option A: | If all the input are same then a carry is generated |
| Option B: | If all of the output are independent of the inputs |
| Option C: | If all of the input are dependent on the output |
| Option D: | If all of the output are dependent on the input |
| | |
| Q21. | In the adder, sum is stored in |
| Option A: | Series |
| Option B: | Cascade |
| Option C: | Parallel |
| Option D: | Registers |
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| Q22. | A barrel shifter is a _____ based Digital circuit. |
| Option A: | Adder |
| Option B: | Encoder |
| Option C: | Multiplexer |
| Option D: | Counter |
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| Q23. | What is ripple carry adder? |
| Option A: | The carry output of the lower order stage is connected to the carry input |

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| | of the next higher order stage |
| Option B: | The carry input of the lower order stage is connected to the carry output of the next higher order stage |
| Option C: | The carry output of the higher order stage is connected to the carry input of the next lower order stage |
| Option D: | The carry input of the higher order stage is connected to the carry output of the lower order stage |
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| Q24. | Electrostatic charge appears when two _____materials come together, transfer charge, and move apart, producing a _____between them. |
| Option A: | Similar, Voltage |
| Option B: | Dissimilar, Current |
| Option C: | Dissimilar, Voltage |
| Option D: | Similar, Current |
| | |
| Q25. | Jitter is the |
| Option A: | Difference between two clock pulses |
| Option B: | Ratio of input transition and output load. |
| Option C: | Difference between required time-arrival time |
| Option D: | Deviation of clock edge from its ideal position. |