Name of Faculty: Kapil Gavali

Title of the paper: A high throughput architecture of DCTQ Processor suitable for FPGA Implementation utilizing Fox Algorithm - International Conference on Inventive Computation Technologies (ICICT 2016), Coimbatore

Title of the paper: VLSI Design of high speed Vedic Multiplier for FPGA Implementation - 2016 International Conference on Engineering & Technology (ICETECH), Coimbatore

Title of the paper: A Parallel Pipelined Adder Suitable for FPGA Implementation - 2018 International Conference on Smart Cities and Emerging

Title of the paper: Simulation of bi-directional

WDM-TDM PON with 5 Gb/s downstream and 2.5 Gb/s Upstream re-modulated Data

based on RSOA -2018 International Conference on Smart Cities and Emerging

Technologies (ICSCET 2018), Mumbai

Title of the paper: Addition Algorithms for VLSI - A review - IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)